

# BJT Process Spread Compensation Utilizing Base Recombination Current in Standard CMOS

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**Abstract**—This letter presents a compensation topology which minimizes the inter-/intra-die spread and proportional-to-absolute-temperature (PTAT) drift of the base-emitter voltage ( $V_{be}$ ) of a bipolar junction transistor (BJT). Without using special devices, the base recombination current from a deep-saturated BJT is utilized in this scheme. Before compensation, the  $V_{be}$  standard deviation (STD) of 15 standalone BJTs measures 3.24 mV at 25 °C with constant external bias currents. After compensation,  $V_{be}$  STD of 30 dies from two batches reduces to 1.8 mV with on-chip bias current. The PTAT drift of  $V_{be}$  as that in typical BJT-based designs are also alleviated.

**Index Terms**—Bipolar junction transistor (BJT) process spread, spread compensation, trimless CMOS voltage reference.

## I. INTRODUCTION

AS THE non-ideality factor of a bipolar junction transistor (BJT) is closer to unity as compared to that of a diode [1, p. 14], it is preferred in precision bandgap voltage reference (BGR) designs. In typical applications, BGR with a temperature coefficient (TC) of  $\sim 30$  ppm/°C (e.g., 6.5 mV error from  $-55$  to  $125$  °C for a 1.2 V output) is sufficient. However, achieving such a performance is a non-trivial task due to the various error sources introduced during silicon fabrication.

BGR error sources such as the amplifier offset, device mismatch and BJT base-emitter voltage ( $V_{be}$ ) curvature can be mitigated by using circuit techniques like chopping, dynamic element matching and signal linearization [1]. Unfortunately, with a pre-defined collector bias, BJT spreads would introduce a proportional-to-absolute-temperature (PTAT) drift in  $V_{be}$  (mainly due to the saturation current  $I_s$  spread) [1, p. 29], which ultimately limits the untrimmed BGR precision. [2] attempted to reduce such PTAT drift by utilizing the reverse current gain ( $\beta_r$ ) of a BJT. Due to the limited correlation between  $\beta_r$  and  $I_s$ , the compensation is sub-optimal with a

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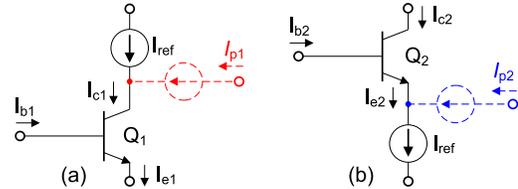


Fig. 1. Two simplified circuit topologies to compensate  $I_s$  spread with compensation currents  $I_{p1,2}$ . (a) Compensation at the collector; (b) compensation at the emitter.

simulated  $V_{be}$  standard deviation (STD) of 2.6 mV at 25 °C. Instead, [3], [4] used pinched base resistors for compensation. However, pinched resistors are no longer supported by modern CMOS processes. This mandates the development of a customized resistor model which is time-consuming and not easy for design transfer.

This letter presents a compensation topology which minimizes the  $V_{be}$  spreads of BJTs under different process conditions. Unlike [3], [4], this scheme only exploits the electrical properties of a standard BJT. After compensation, the measured  $V_{be}$  STD reduces from 3.24 mV to 1.8 mV at 25 °C, and the PTAT drift in  $V_{be}$  is also shown to be well-suppressed, demonstrating the feasibility of the proposed scheme for designing trimless BGRs.

## II. BIPOLAR SPREAD AND COMPENSATION

### A. Process Spread of BJT

The base-emitter voltage of a BJT biased in its forward-active region is [1]

$$V_{be} = V_T \cdot \ln\left(\frac{I_c}{I_s}\right) \quad (1)$$

where  $V_T$  is the thermal voltage;  $I_c$  and  $I_s$  are the BJT collector bias current and saturation current, respectively. Since  $I_s \propto N_b^{-1}$  and  $N_b$  cannot be precisely controlled during fabrication ( $N_b$  is the BJT base doping concentration) [1, p. 16],  $I_s$  can exhibit as large as  $\pm 30\%$  inter-/intra-die variation, which introduces a spread of  $\pm 10.5$  mV in  $V_{be}$  at 125 °C. From (1), in order to maintain  $V_{be}$  of different dies to be the same at the reference temperature  $T_r$ ,  $I_c$  needs to track the process spread of  $I_s$ .

Fig. 1 shows two basic  $I_s$  spread compensation topologies for an NPN BJT, where  $I_{p1,2}$  are the compensation currents. To minimize  $V_{be}$  variation,  $I_{p1,2}$  need to satisfy two conditions. Firstly, they must have strong correlation with  $I_s$ . Secondly, since the spread of  $I_s$  increases with temperature [1, p. 21], the spread of  $I_{p1,2}$  needs to increase with temperature as well to achieve compensation over a wide temperature range.

### B. Compensation Principle

In this work, a BJT operating in its deep-saturation region (with tens of mV collector-emitter voltage  $V_{ce}$ ) is exploited

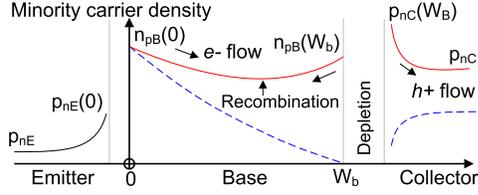


Fig. 2. Minority carrier density profile of an NPN BJT biased in its forward-active (dashed line) and deep saturation (solid line) regions [5, pp. 10–17].  $x = 0$  is the edge of the BE junction depletion layer.  $W_b$  is the width of the base neutral region.  $n_{pB}(W_b)$  represents the n-type carrier in the p-type base region at  $x = W_b$ .

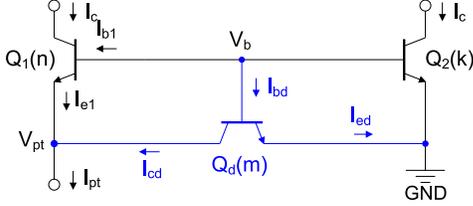


Fig. 3. The proposed on-chip BJT spread compensation topology utilizing a deep-saturated BJT  $Q_d$ .

for  $I_s$  spread compensation. Fig. 2 shows the minority carrier density of such an NPN BJT [5, pp. 10–17], where the minority carrier (e-) density in the base region is high but the density gradient is small since  $V_{be}$  and  $V_{bc}$  are comparable. As a result, the electrons are trapped in the base region and strong electron-hole recombination occurs. The induced recombination current  $I_r$  can be expressed as the overall minority carrier charge  $Q_n$  and its life time  $\tau_b$  in the base region

$$I_r = \frac{Q_n}{\tau_b} \approx \frac{AqW_b n_i^2}{2N_b \tau_b} (e^{V_{bc}/V_T} + e^{V_{bc}/V_T}) \propto \frac{I_c}{\tau_b} \quad (2)$$

where  $A$  is the BJT emitter area,  $W_b$  is its base width,  $n_i$  is the intrinsic carrier concentration and  $I_c$  is the collector bias current of a BJT that generates the base bias voltage for this deep-saturated BJT. Based on the concentration-dependent Shockley-Read-Hall (SRH) model [6], for  $N_b$  higher than  $10^{17}/\text{cm}^3$ ,  $\tau_b \propto N_b^{-1}$ . As a result,  $I_r \propto I_s^{-1}$  (since  $I_s \propto N_b^{-1}$ ), and this strong correlation between  $I_r$  and  $I_s$  is exploited to perform BJT process compensation. If  $I_c$  is designed to have a positive TC,  $I_r$  then satisfies the two requirements of the compensation current  $I_{p2}$  in Fig. 1 (b).

The proposed compensation topology is shown in Fig. 3, in which  $V_b$  is the target  $I_s$  spread insensitive voltage.  $Q_{1,2}$  are matched vertical BJTs working in their forward-active regions, with an emitter area ratio of  $n:k$  and the same collector current.  $Q_d$  is the deep-saturated BJT with an emitter area of  $m$  units. Its collector current  $I_{cd}$  contains the aforementioned recombination current  $I_r$  for  $I_s$  spread compensation. To maintain  $Q_d$  in its deep-saturation region,  $n:k$  is sized to be 4:2 (the  $V_{ce}$  of  $Q_d$  is  $V_{pt} = V_T \cdot \ln(n/k)$ , about 24 mV at 125 °C). In Fig. 3, by including  $I_s$  and  $I_{cd}$  spread,  $V_b$  is expressed as

$$V_b \approx V_T \cdot \ln \frac{I_{pt} - (I_{cd}|_{\text{Ideal}} + \Delta I_{cd})}{(1 + \alpha) \cdot I_s|_{\text{Ideal}}} \quad (3)$$

where  $\alpha$  is the  $I_s$  spread coefficient and  $\Delta I_{cd}$  represents the variation of  $I_{cd}$ . For optimal compensation,  $\Delta I_{cd}$  equal to  $-\alpha \cdot (I_{pt} - I_{cd}|_{\text{Ideal}})$ . Worthly to mention that, without

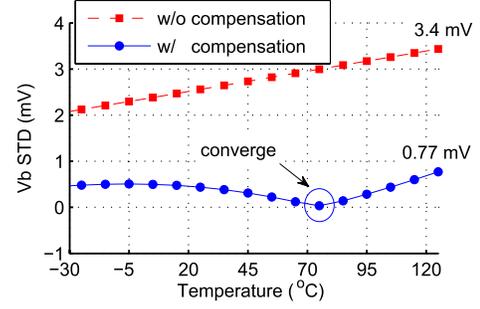


Fig. 4. Simulated STD of  $V_b$  (Fig. 3) with and without using  $Q_d$  for compensation at different temperatures from 250 monte-carlo runs.

compensation,  $|\partial V_b / \partial I_s| = V_T / I_s$ ; while after compensation

$$\left| \frac{\partial V_b}{\partial I_s} \right| \approx \frac{V_T}{I_s} \cdot \left| \frac{b I_r}{I_c |_{\text{Ideal}} + b I_r} - 1 \right| < \frac{V_T}{I_s} \quad (4)$$

where  $b$  (a complex function of BJT bias condition and process [8]) is the fraction of  $Q_d$ 's base recombination current that flows to its collector. From (4),  $V_b$  is less sensitive to  $I_s$  after introducing the recombination current  $I_r$ .

The design is implemented in the GlobalFoundries 0.18  $\mu\text{m}$  CMOS process. A moderate PTAT bias with  $I_{pt} = 100$  nA at 25 °C is adopted for low power consumption. For effective compensation,  $m$  is sized to be 6 units ( $5 \mu\text{m} \times 5 \mu\text{m}$  unit area), with  $I_{cd}|_{\text{Ideal}}$  and  $\Delta I_{cd}$  equal to 43.6 nA and  $\mp 18.6$  nA at the fast and slow BJT corners at 25 °C, respectively. Fig. 4 shows the STD of  $V_b$  with and without  $Q_d$  compensation from 250 monte-carlo simulation runs. It can be observed that  $V_b$  exhibits a PTAT drift without compensation. After compensation, the PTAT drift in  $V_b$  is suppressed and its maximum STD is reduced by 4.5 $\times$  from 3.4 mV to 0.77 mV, with ideal compensation achieved at 70 °C.

### III. VERIFICATION IN STANDARD CMOS

The complete BJT spread compensation circuitry is shown in Fig. 5 and Fig. 6 shows its die photo.  $Q_{1,2,d}$  form the BJT core.  $M_{p1-4}$  and  $M_{n1,2}$  are for circuit start-up.  $M_{p5-7}$  and a native transistor  $M_{\text{nat}}$  provide the BJT collector and base currents.  $M_{p8-10}$  and  $M_{n3-5}$  form a current comparator and error amplifier to generate a pseudo-supply  $V_s$  and to equalize  $V_{1,2}$ , which ensures  $Q_{1,2}$  collector current to be the same [7].  $R_p$ ,  $M_{p11,12}$  and  $M_{n6,7}$  form a peaking current source to bias the error amplifier. In Fig. 5,  $Q_{1,2,d}$ ,  $M_{p6,7}$  are common-centroid laid out to minimize their mismatches induced inter-/intra-die  $V_{be}$  spread. Meanwhile,  $R_{pt}$  used to generate  $I_{pt}$  is a composite resistor formed by 6 different resistor types to reduce its overall resistance variation [9].

The  $V_{be}$  STD of 15 standalone BJTs measures 3.24 mV at 25 °C using external bias current. Fig. 7 shows the measured compensated  $V_b$  from two batches with on-chip biasing. The corresponding STD reduces to only 1.8 mV at 25 °C [Fig. 8 (a)], which is about twofold reduction compared with that without compensation [Fig. 8(b)]. By using an external  $R_{pt}$  of 180 k $\Omega$  to isolate the resistor spread, the  $V_b$  STD further reduces to 1.5 mV at 25 °C. The  $V_{be}$  spread of the proposed scheme is 1.4 $\times$  and 1.7 $\times$  smaller than prior arts that use reverse current gain [2] (simulated) or pinched base resistor [3] (simulated) for compensation, respectively. In contrast to [3] and [4] which still exhibit inter-/intra-die

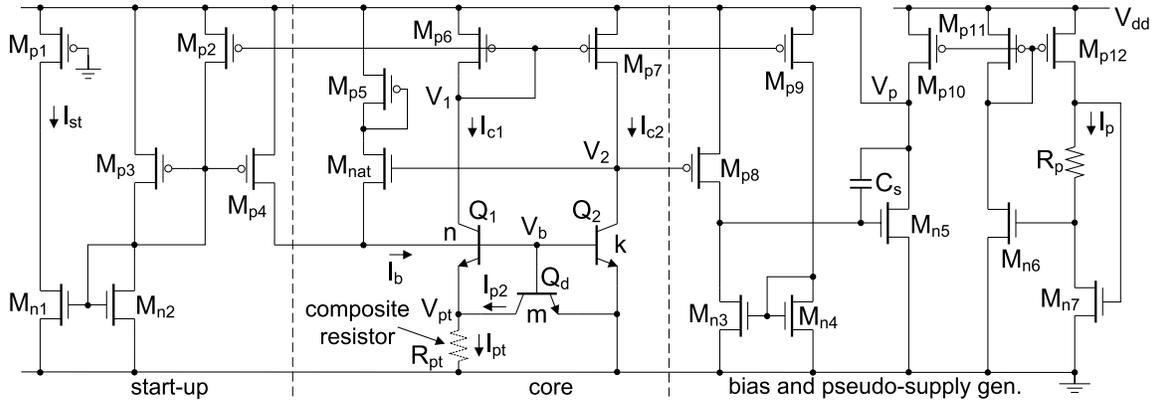
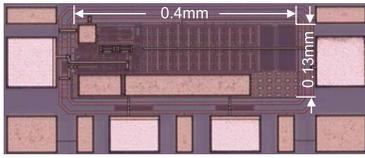
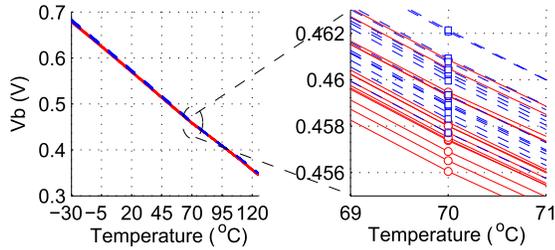
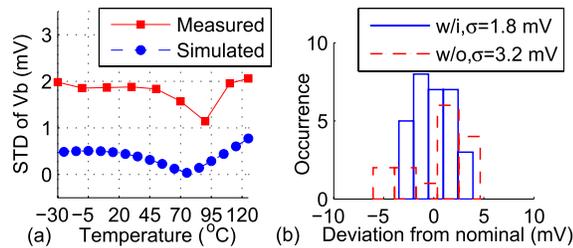


Fig. 5. Schematic of the proposed BJT spread compensation circuitry.

Fig. 6. Microphotograph of the test chip in 0.18  $\mu\text{m}$  CMOS.Fig. 7. Measured  $V_b$  as a function of temperature of 30 dies from two batches (zoom in at 70  $^{\circ}\text{C}$ ).Fig. 8. Measured (a) STD of  $V_b$  at different temperatures and (b)  $V_b$  deviation histogram with and without compensation (at 25  $^{\circ}\text{C}$ ).

PTAT spreads, the measured  $V_b$  STD is 2 mV at  $-30^{\circ}\text{C}$  and  $125^{\circ}\text{C}$ , but converges to 1.1 mV at  $85^{\circ}\text{C}$ . This is consistent with SPICE simulation, demonstrating the feasibility of the proposed scheme for  $V_{be}$  PTAT spread suppression. However,  $I_{pt}$  can deviate from its nominal value due to various error sources including  $R_{pt}$  spread,  $Q_{1,2}$ ,  $M_{6,7}$  mismatches etc. The optimal compensation current  $I_{cd}$  in (3) then varies, which alters the optimal compensation temperature and increases the uncertainty of  $V_b$ . Moreover, in the BJT model, the silicon band gap energy  $E_g$  is constant without modeling its temperature dependency and doping induced band gap

shift [8, p. 15–258], which degrades the modeling precision as well and enlarges the discrepancy between SPICE and silicon measurements.

#### IV. CONCLUSION

A BJT process spread compensation method using the base recombination current of a deep-saturated BJT is presented. A detailed compensation current generation principle is outlined, with the dominant error sources of the BJT  $V_{be}$  spread explained. We also proposed circuit topology that can minimize the inter-/intra-die  $V_{be}$  variation. Measurement results from the prototype chip fabricated using the GlobalFoundries 0.18  $\mu\text{m}$  standard CMOS process show about twofold reduction in  $V_{be}$  spread after compensation. It can be concluded that the proposed scheme simplifies the circuit design compared to prior arts and is compatible to mainstream CMOS processes.

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