

A Wide Input Range Dual-Path CMOS Rectifier for RF Energy Harvesting

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Abstract—This brief presents a dual-path CMOS rectifier with adaptive control for ultrahigh-frequency (UHF) RF energy harvesters. The input power range with high power conversion efficiency (high PCE) of the rectifier is extended by the proposed architecture, which includes a low-power path and a high-power path. The dual-path rectifier with an adaptive control circuit is fabricated in a 65-nm CMOS process. Operating at 900 MHz and driving a 147-k Ω load resistor, the measured PCE of this work can be maintained above 20% with an 11-dB input range from -16 to -5 dBm, while only an 8-dB input range can be achieved with traditional single-path rectifiers. A sensitivity of -17.7 dBm is measured with 1-V output voltage across a capacitive load.

Index Terms—CMOS rectifier, cross-connected (CC) rectifier, RF energy harvesting, ultrahigh frequency (UHF), wireless power transfer (WPT).

I. INTRODUCTION

ENERGY harvesting has become increasingly important for a wide range of applications that include the wearable electronic devices, radio frequency identification (RFID), Internet of Things, and biomedical implanted devices [1]–[5]. Multiple energy sources, such as sunlight, vibration, thermal, and RF energy, are potential candidates for various energy-harvesting applications. While some sources are limited by the application scenarios, the density of wireless devices keeps increasing rapidly worldwide in this decade. And most of the communication systems operate in the ultrahigh-frequency (UHF, 300 MHz to 3 GHz) ISM bands. Thus, abundant RF energy is readily available in the ambient, and multiband RF energy can be harvested simultaneously [6].

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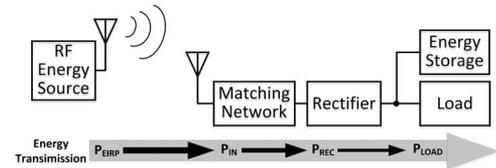


Fig. 1. Generic far-field WPT system.

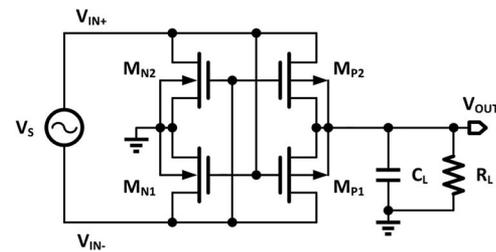


Fig. 2. Schematic of a single-stage CC CMOS rectifier.

Fig. 1 shows a conceptual far-field wireless power transfer (WPT) system between an RF energy source and an RF energy harvester. In this system, the RF energy source could be a base station or a cellular phone, or even a Wi-Fi router. Then, the incident RF power is received by the antenna of the energy harvester and fed to a matching network. After that, a rectifier converts the RF power to dc power for the energy storage device and the load.

Diode drop is one of the main constraints that limits the low-voltage operation of the rectifiers. The cross-connected (CC) CMOS rectifier structure [7], as shown in Fig. 2, is a commonly used topology for its low-voltage and autoswitching characteristics. It has been demonstrated in [1] that the voltage conversion ratio of the CC topology could be larger than 80% when the input amplitude of the rectifier was higher than 150 mV. However, a high leakage current will occur at high input amplitude conditions because the pMOS and nMOS will be turned on simultaneously during the transition period, which is a similar problem to the shoot-through current of a CMOS inverter. To achieve better sensitivity, larger transistor sizes are required for the rectifier, which will cause more reverse leakage current that limits the efficiencies at high input power. Larger transistor size will also increase the parasitic loss during the step-up conversion [8]. Thus, the CC rectifier evidently provides higher peak power conversion efficiency (PCE) than the Dickson rectifier [9]. However, its high-PCE range is narrow due to the aforementioned leakage current problem.

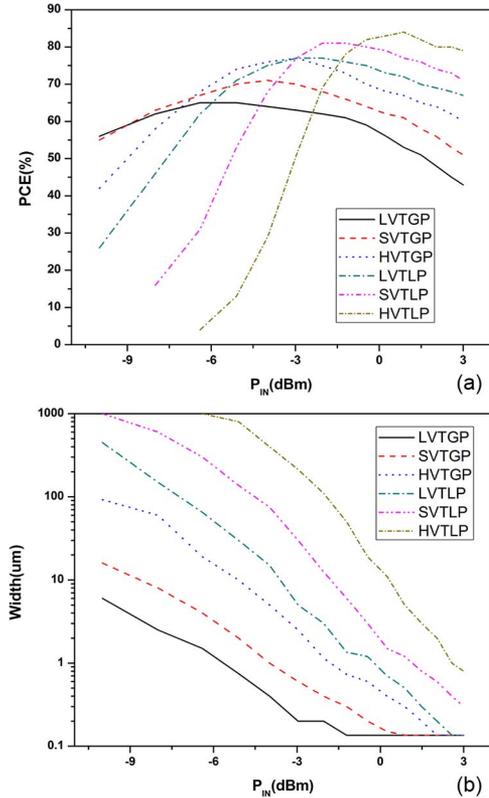


Fig. 3. Simulated (a) PCE versus P_{IN} and (b) the nMOS widths used to obtain a peak PCE at the corresponding P_{IN} for six transistor types in a 65-nm process.

In this brief, to extend the high-PCE range, a dual-path rectifier based on the CC structure is presented. The operation principle of the proposed dual-path rectifier is introduced in Section II. Section III shows the circuit implementation. Section IV presents the experimental results and discussions. Finally, a conclusion is drawn in Section V.

II. OPERATION PRINCIPLE OF THE PROPOSED RECTIFIER

As discussed earlier, the single-path CC topology can improve the PCE for only a narrow predefined operation range. To investigate the performances of the CC rectifier, the simulated PCEs versus the input power P_{IN} with six types of transistors available in a 65-nm CMOS process with the same transistor sizes are given in Fig. 3(a). The six types of transistors include the low threshold (LVT), standard threshold (SVT), and high threshold (HVT) of the general-purpose (GP) transistors and also the corresponding low-power (LP) version transistors. Meanwhile, the widths of the pMOS are set to be two times that of the nMOS, and all the channel lengths are the minimum. In addition, Fig. 3(b) shows the nMOS widths that are used to obtain a peak PCE at the corresponding P_{IN} . The simulation results show that the peak PCE could be achieved at different P_{IN} , by selecting a specific type of transistor and an optimum size. For example, the maximum PCEs achieved at $P_{IN} = -8$ dBm and $R_L = 100$ k Ω , with nMOS LVTGP transistors having $W = 2.5$ μm or LVTLP transistors with $W = 150$ μm , are 62% and 46%, respectively. Generally, low- V_{TH} transistors can achieve better PCE at lower P_{IN} , and high- V_{TH} transistors can achieve a higher peak PCE.

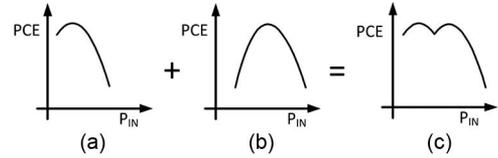


Fig. 4. Efficiencies of the conventional rectifier (a) optimized at low power and (b) optimized at high power and (c) the PCE of the proposed dual-path rectifier.

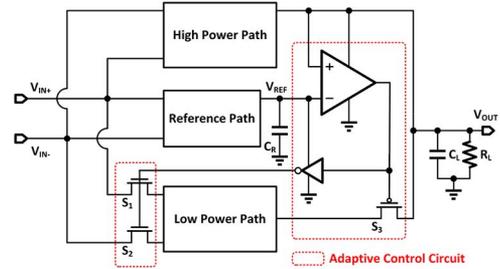


Fig. 5. System architecture of the dual-path rectifier.

Fig. 4 shows the basic conceptual idea used in this work. Fig. 4(a) shows the high-PCE range for a conventional single-path rectifier that is optimized at a low input power, and Fig. 4(b) shows the range that is optimized at a high input power. Apparently, only a narrow high-PCE input power range can be achieved for a single path. On the other hand, Fig. 4(c) shows that the high-PCE range of the proposed dual-path rectifier is extended by combining both curves in Fig. 4(a) and (b). Now, the questions are how to automatically select the two paths with negligible power consumption, and how to effectively disable one path without affecting the other.

The block diagram of the proposed rectifier is shown in Fig. 5. The dual-path rectifier consists of a low-power path using LVTGP transistors for high PCE at low input power and also for better input sensitivity, a high-power path using LVTLP transistors designed for high PCE at high input power, a reference path that generates a threshold voltage for the automatic path selection, and three switches S_1 through S_3 to enable/disable the low-power path. Thus, the system can automatically choose the appropriate path, according to the input power level to achieve a wider high-PCE range. Of course, the thick-oxide input/output (IO) devices can also be a choice for the high-power path. One problem is that the input impedance of the rectifier with IO devices would vary more from that of the rectifiers all using the thin-oxide devices. This makes the matching network more difficult to satisfy the two paths without additional tuning control.

The reference path is also a CC rectifier path using the same type of transistors and the same number of stages as the high-power path. However, it only drives the input of the comparator and an inverter. Then, it can provide a relatively high voltage, when comparing with the high-power path, which drives a resistive load. The comparator with built-in offset compares the V_{REF} and V_{OUT} to select the path. As shown in Fig. 6(a), when V_{OUT} is low and V_{REF} is high, the comparator will output “0” although its supply is low, and the inverter will output “1” accordingly. Then, the switches S_1 , S_2 , S_3 are turned on, and

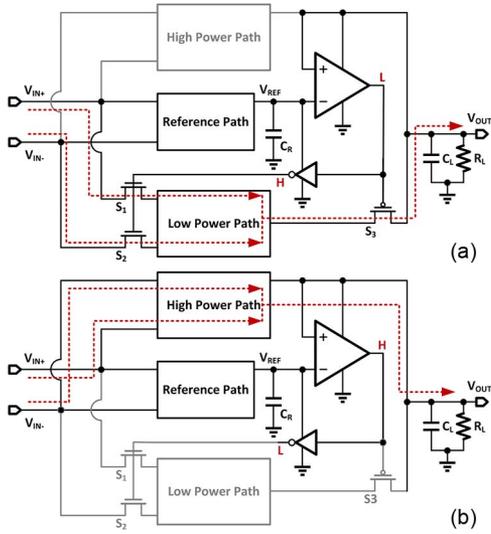


Fig. 6. Proposed rectifier with (a) low-power path operating state and (b) high-power path operating state.

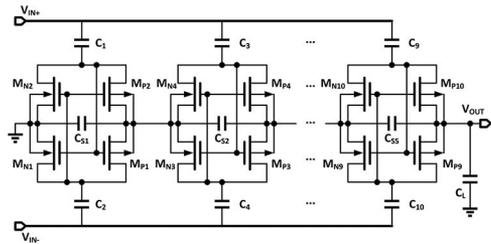


Fig. 7. Schematic of the five-stage CC rectifier.

the low-power path is enabled. Note that the high-power path exhibits high input impedance, and does not need to be disabled when the low-power path is operating, since the low P_{IN} is not powerful enough to switch on the LVTLP transistors. On the contrary, the low-power path needs to be disconnected at high-power conditions; otherwise, the low-power path will generate a large reverse leakage current that limits the V_{OUT} . When the V_{OUT} is higher than V_{REF} , the comparator will output “1,” then the low-power path is disabled and the high-power path starts to operate.

III. CIRCUIT IMPLEMENTATION

A. Rectifier Design

As the input amplitude is quite low in the RF energy-harvesting case, with a passive impedance matching network for voltage boosting, five stages are used to generate 1 V at the input power of -16 dBm. Although it might be considered that higher efficiency can be achieved with less conversion stages, it has been shown that the maximum achievable efficiency can be maintained, even if the number of stages increases [10].

Fig. 7 shows the five-stage CC rectifier for the low-power path. The peak PCE can be achieved at an input power of -16 dBm with LVTGP transistors. For the high-power path, the schematic is almost the same, except that C_1 and C_2 are removed to provide a dc bias for V_{IN+} and V_{IN-} . The peak PCE can be achieved at -10 dBm with LVTLP transistors. In this

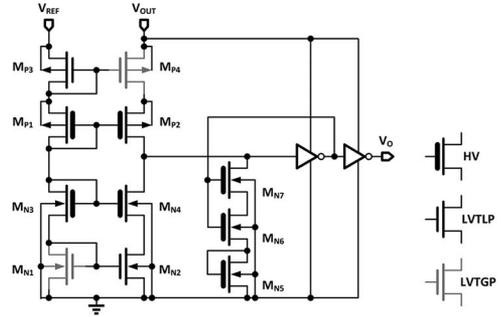


Fig. 8. Schematic of the comparator for adaptive control.

brief, the width of the nMOS transistors is $40 \mu\text{m}$ divided by 40 fingers with the minimum channel length for the high-power path, whereas that of the low-power path is $10 \mu\text{m}$ divided by ten fingers. With a deep n -well process, each stage inhabits in its own p -well to eliminate the body effect such that the V_{TH} , and consequently the PCE peak point of each stage, is kept the same. In addition, the dc output of each stage needs to be stable during normal operation. Otherwise, large output ripple will be observed at V_{OUT} . Thus, C_{Sn} ($n = 1, 2, \dots, 5$) of 600 fF each is added.

To mimic the operation of the main path and generate a reasonable reference voltage V_{REF} , the five-stage reference path also uses the structure in Fig. 7. Since the reference path only drives a tiny load that is mainly capacitive, the width of the nMOS is only $4 \mu\text{m}$. Thus, the power consumption of the reference is negligible.

B. Adaptive Control Circuit

Since the harvested power is very limited, one of the main issues to take into account in the controller design is to avoid extra power consumption. The common-gate input comparator, as shown in Fig. 8, is the main part of the adaptive control circuit. The comparator draws current from both outputs of the high-power path and the reference path. For the left branch, V_{REF} is divided into four cascoding gate-to-source voltages, which are derived from two high-voltage (HV), one LVTLP, and one LVTGP transistors. When operating in the subthreshold region, the current consumption of the comparator exhibits exponential growth with respect to V_{REF} , and thus is negligible at low input power conditions. In addition, the long-channel HV devices that have lower current conduction capability are used to further reduce the current consumption. When $V_{OUT} = 1$ V, the comparator in the simulation only consumes 187 pA. Even in the worst case of $V_{OUT} = 3$ V, it is 457 nA, which only counts for 2.2% of the rectifier output current.

The reason for using both LVTLP and LVTGP transistors in the comparator is that the V_{TH} difference between these two types naturally generates an offset voltage for the comparator to appropriately select the path because the output voltages of dual paths are functions of the V_{TH} of the transistors used in each path. Moreover, the offset would track the process variations for the dual paths using these two types of transistors. Thus, the trip point of the comparator is a complex function of V_{TH} and load condition, and this is a compromise for path selection.

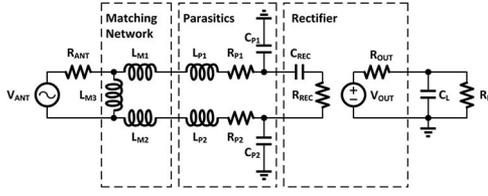


Fig. 9. Block diagram of the RF energy harvester.

Ignoring the offset for the time being, when V_{OUT} is higher than V_{REF} , more current will pass through M_{P4} and M_{P2} , and it will pull up the comparator output V_O to switch the rectifier paths, and vice versa. In addition, a hysteresis is generated by M_{N6} and M_{N7} which will be turned on when V_O is low.

C. Impedance Matching Network Design

In this design, an RF input power source with 50- Ω output impedance is employed for measurement, as shown in Fig. 9. The power source can be modeled as an equivalent voltage source with the amplitude V_{ANT} in series with a resistance R_{ANT} . V_{ANT} can be calculated from the following equation [11]:

$$V_{ANT} = \sqrt{8 \times R_{ANT} \times P_{AV}} \quad (1)$$

where P_{AV} is the available input power at the antenna. For example, the V_{ANT} with -20 dBm available power from a 50- Ω antenna is only 63.25 mV, which is considered as low for the rectifier to operate. Then, to generate a sufficiently large input voltage to cater for the rectifier is one of the major issues to operate at low input power. Therefore, the impedance matching circuit is critical to optimize the power transfer through the power chain. The input impedance of the rectifier is determined not only by its own input capacitance and resistance but also by the parasitic capacitance and inductance from the bond pads, bond wires, and the printed circuit board (PCB) traces. Moreover, the effective input impedance varies with the input power due to the large-signal characteristics of the rectifier. Both C_{P1} and C_{P2} are 250-fF extracted parasitic capacitors of the bonding pad. A single bond wire to the PCB is modeled with a 2-nH inductor in series with a 0.3- Ω resistor. Then, the simulated input impedance Z_{IN} seen from the PCB into the chip at 300-mV input amplitude and 900-MHz condition is $18 - j190 \Omega$, which is equivalent to an 18 Ω resistor in series with a 1.97-pF capacitor. Thus, a shunt-series inductor topology is chosen for the matching network. Off-chip L_{M1} , L_{M2} , and L_{M3} are used to cancel the capacitive term of the rectifier. In addition, the matching network is used as a passive voltage boosting circuit to improve the sensitivity. Then, the input amplitude of the rectifier can be calculated using the following equation [12]:

$$V_{IN} = \frac{V_{ANT}}{2} \sqrt{1 + Q^2}. \quad (2)$$

In this setup, a P_{AV} of -15.4 dBm can provide a V_{IN} of 300 mV with a V_{ANT} of 107 mV. As discussed in [1], the sensitivity, or

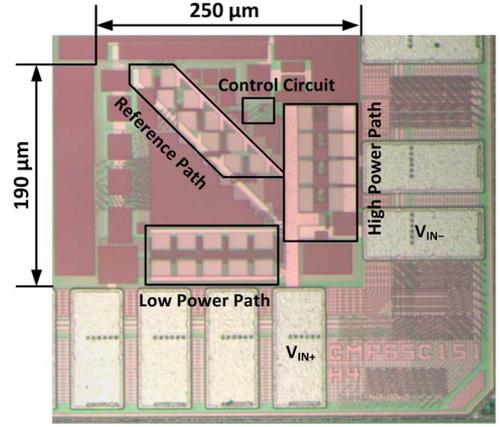
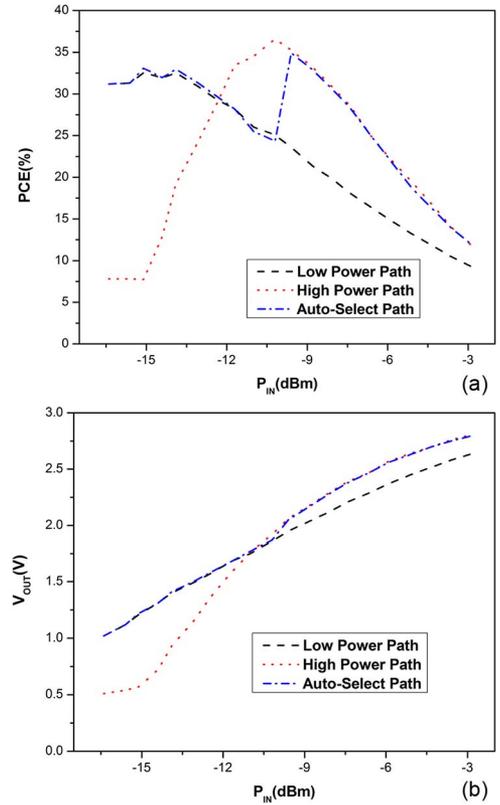


Fig. 10. Chip micrograph of the proposed dual-path rectifier.


 Fig. 11. Measured (a) PCE and (b) V_{OUT} versus P_{IN} with $R_L = 147$ k Ω .

the minimum required P_{AV} for a desired V_{IN} , can be written as

$$P_{AV,\min} = \left(\frac{R_{ANT} + R_{REC}}{\frac{1}{\omega C_{REC}}} \right)^2 \frac{V_{IN}^2}{8\eta_A R_{ANT}}. \quad (3)$$

It indicates that reducing the input capacitance C_{REC} can effectively improve the sensitivity, while η_A is the radiation efficiency that varies with the antenna size.

IV. EXPERIMENTAL RESULTS AND DISCUSSIONS

The proposed dual-path rectifier is fabricated in a 65-nm CMOS process. Fig. 10 shows the micrograph of the chip.

TABLE I
PERFORMANCE SUMMARY AND COMPARISON WITH PREVIOUS WORKS

| Publication | This work | Yi '07 [10] | Le '08 [13] | Papotto '11 [14] | Stoopman '14 [1] |
|--------------------------------|---------------------------|-----------------------|--------------------------|---------------------------|--------------------------|
| Technology | 65nm | 0.18 μm | 0.25 μm | 90 nm | 90 nm |
| Effective area | 0.048 mm ² | 0.084 mm ² | 0.4 mm ² | 0.19 mm ² | 0.029 mm ² |
| Frequency | 900 MHz | 900 MHz | 906 MHz | 915 MHz | 868 MHz |
| No. of Stages | 5 | 24 | 36 | 17 | 5 |
| Peak PCE @ R_L | 36.5% @ 147 k Ω | 26.5% @ N.A. | 30% @ 0.33 M Ω | 16.1% @ 0.5 M Ω | 40% @ 0.33 M Ω |
| Sensitivity ($R_L = \infty$) | -17.7 dBm | N.A. | -22.6 dBm | -24 dBm | -27 dBm |
| High-PCE Range* | 11 dB | N.A. | 8 dB** | N.A. | 12 dB** |

* PCE above 20%

** Estimated from the figure

The effective area excluding the pads is $250 \times 190 \mu\text{m}^2$. The chip is wire bonded to a FR4 PCB with chip-on-board (COB) setup, and this is tested with a single-tone sinusoidal wave with $50\text{-}\Omega$ source impedance at the frequency of 900 MHz. Since the structure of the rectifier is differential, the PCB ground (floating ground) and the ground of the signal generator (the earth) are separated, and the value of the off-chip C_L is 100 nF.

To evaluate the two paths separately, two additional control pins Set_LP and Set_HP can be used to enable/disable the low-power or high-power path off-chip. When both Set_LP and Set_HP are tied to high voltage, the system will operate with automatic path selection.

Fig. 11(a) shows the measured PCE of the RF energy harvester including matching network versus the input power P_{IN} with a step size of 0.5 dB. Measurement results show that the PCE above 25% for the low-power path can be maintained from -16 to -11 dBm, and from -12 to -7 dBm for the high-power path. The results also show that the peak PCEs for the low-power and high-power paths are 32.5% and 36.5% at the input power of -14 and -10 dBm, respectively. When the dual-path rectifier is selected automatically by the adaptive control circuit, the PCE is higher than 20% with P_{IN} ranging from -16 to -5 dBm, maintaining 11-dB input power range. Although the measured path-switching point does not happen to be the ideal switching point due to process variations, the PCE curve with autoselect path is still improved compared to that of single paths. Fig. 11(b) shows that the output voltage of the high-power path is higher than the low-power path, starting from -11 dBm. The minimum P_{IN} required to charge up the system with 1-V output is measured to be -16 dBm, with a 147-k Ω load, and a sensitivity of -17.7 dBm is measured for 1-V output with capacitive load only. In this prototype, certain sensitivity is sacrificed for the potential wider high-PCE range.

Table I shows a performance summary and comparison with previous works. This work demonstrated a better or comparable input power range of 11 dB, in which the PCE can be maintained above 20%. Since the input impedance of the rectifier would vary with P_{IN} that affects the PCE, a more flat PCE curve is expected with a capacitor bank for impedance matching, as demonstrated in [1].

V. CONCLUSION

This brief presents a UHF RF energy harvester that features an efficient dual-path structure with adaptive autoselect control

that maintains high PCE for a wide range. A common-gate input comparator with hysteresis is proposed to switch the path with little power overhead. Implemented in a 65-nm CMOS technology, a sensitivity of -17.7 dBm for 1-V output with a capacitive load is measured. The above 20% PCE range of the proposed RF energy harvester can be maintained from -16 to -7 dBm with a range of 11 dB, while the single-path rectifiers can only maintain the high-PCE range for an 8-dB range.

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