DCM operation analysis of 3-level boost converters

Yi-Wei Tan, Chi-Seng Lam✉, Sai-Weng Sin, Man-Chung Wong, Seng-Pan U. and Rui Paulo Martins

The 3-level boost (3LB) converters have the characteristics of higher-voltage conversion ratio and efficiency, lower inductor current ripples, output voltage ripples and voltage stresses on switches when compared with the conventional boost converters in continuous conduction mode (CCM). When implemented into an integrated circuit, the 3LB converter discontinuous conduction mode (DCM) operation cannot be avoided due to a smaller inductance. Its DCM operation analysis is deduced including CCM/DCM boundary, DCM voltage gain and DCM small signal transfer function. The deduced DCM operation theory is verified using MATLAB and Cadence, to obtain a feasible DCM closed-loop controller design in future.

Introduction: Many portable products as MPEG-3 players, personal digital assistants, wearable devices, etc., call for voltage boosting DC–DC converters. For such applications, the output voltage ripple, conversion ratio and noise must be considered. For the conventional boost converters, their output currents pulsate, thus leading to large output voltage ripples. A 3-level boost (3LB) converter for continuous conduction mode (CCM) operation is proposed in [1–3] to reduce inductor current ripples, output voltage ripples and voltage stresses on switches, thus yielding a higher conversion ratio and efficiency. Both 3LB and boost converters have the same CCM voltage gain and small signal transfer function for the closed-loop controller design [4]. When 3LB converter is designed into an integrated circuit (IC), its discontinuous conduction mode (DCM) operation, cannot be avoided. This Letter aims to present its DCM operation analysis, which has a surprisingly different DCM voltage gain and small signal transfer function.

3LB converter and its ideal equivalent circuits for DCM: Fig. 1 shows the proposed 3LB converter IC topology in DCM, where V_{IN}, V_O and V_{REF} are the DC input, output and reference voltages; C_f and V_{Cf} are the flying capacitor and its voltage ($V_{Cf} = 0.5V_O$); L and C are the inductor and capacitor; R_{load} is the load resistor; I_{IN}, I_{Load}, I_{cf}, I_L and I_C are the input, load, flying capacitor, inductor and capacitor currents; S_{1-5} are the different operation states; and M_{1-4} are the power transistor switches. A compensator is used to obtain a stable and fast control loop. A pulse-width modulator (PWM) generates V_{Toppwm}, V_{Midpwm} and V_{Botpwm} signals. The V_{Top}, V_{Mid} and V_{Bot} signals via the level shifter, non-overlapping and driver circuits are used to control those transistor switches [5], and zero current detector (ZCD) represents the zero current detector to trigger S_5. Fig. 2 shows the 3LB converter idealised inductor voltage V_L and current I_L waveforms for DCM, where D is the duty ratio. When $0 < D < 0.5$, it is operating as in Fig. 2*a*. When $0.5 < D < 1$, it is operating as in Fig. 2*b*. For CCM, S_5 does not exist; its CCM voltage gain is $M_{VDC\_CCM} = V_O/V_{IN} = 1/(1-D)$ [1–3], which is exactly the same as the boost converter [4]. Also, they have the same CCM small signal transfer function.

Boundary between CCM and DCM of 3LB converter: From Fig. 2, the boundary between CCM and DCM can be derived when $D_3 = 0$. From Fig. 2 and M_{VDC_CCM}, the peak inductor current can be obtained as (1) and (2), and then the average DC input/inductor current at the CCM/DCM boundary can be determined as $I_{INB} = I_{LB} = I_{Lpk}/2$, with

$$I_{Lpk} = \frac{1}{f_s L}(V_{IN} - 0.5V_O)D = \frac{V_O}{f_s L}\left(0.5D - D^2\right), \quad 0 < D < 0.5 \quad (1)$$

$$I_{Lpk} = \frac{1}{f_s L}V_{IN}(D - 0.5) = \frac{V_O}{f_s L}\left(1.5D - D^2 - 0.5\right), \quad 0.5 < D < 1 \quad (2)$$

where f_s is the switching frequency. From Fig. 1, the DC load current is

$$I_{Load} = \frac{V_o}{R_{Load}} = \frac{V_{IN}}{V_o}I_L \quad (3)$$

where $I_{IN} = I_L$. With M_{VDC_CCM}, I_{INB} and (3), the load current I_{LoadB} and load resistance R_{LoadB} at the boundary are deduced as (4) and (5). Fig. 3 shows the normalised load current $I_{LoadB}/(V_{out}/4Lf_s)$ and load resistance $R_{LoadB}/4Lf_s$ at the CCM/DCM boundary as a function of D

$$I_{LoadB} = \frac{V_O D(1-D)(1-2D)}{4Lf_s}, \quad R_{LoadB} = \frac{4Lf_s}{D(1-D)(1-2D)}, \quad 0 < D < 0.5 \quad (4)$$

$$I_{LoadB} = \frac{V_O(2D-1)(1-D)^2}{4Lf_s}, \quad R_{LoadB} = \frac{4Lf_s}{(2D-1)(1-D)^2}, \quad 0.5 \le D \le 1 \quad (5)$$

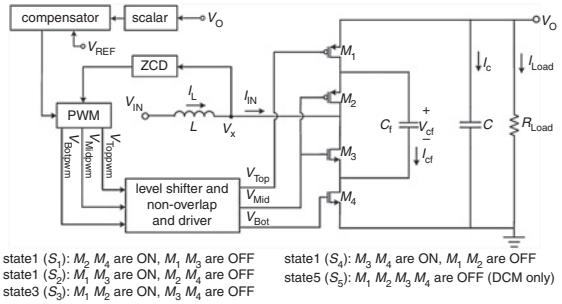

Fig. 1 *Proposed 3LB converter IC topology for DCM*

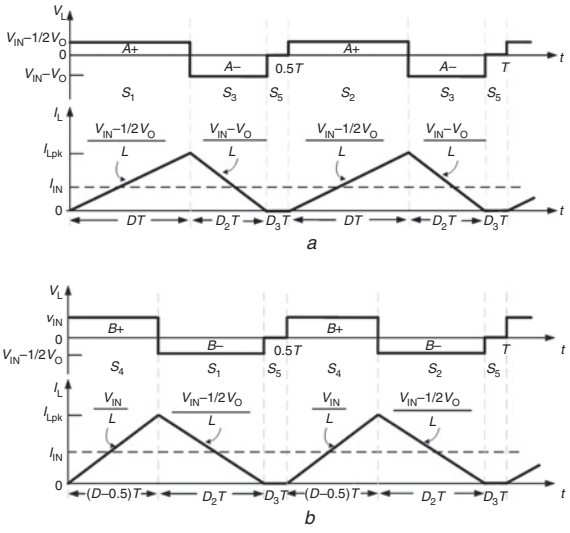

Fig. 2 *3LB converter idealised V_L and I_L waveforms for DCM*
a When $0 < D < 0.5$
b When $0.5 < D < 1$

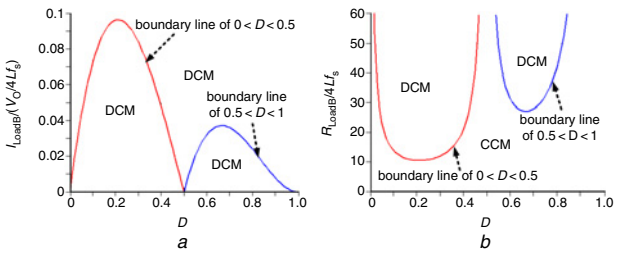

Fig. 3 *Normalised load current and load resistance at CCM/DCM boundary as function of D for 3LB converter*
a $I_{LoadB}/(V_O/4Lf_s)$ against D
b $R_{LoadB}/4Lf_s$ against D

DC voltage transfer function of 3LB converter for DCM: From Fig. 2, the average DC inductor current can be deduced as (6) and (7)

$$I_L = \frac{1}{T}\int_0^T i_L(t)\,dt = (D + D_2)I_{Lpk}, \quad 0 < D < 0.5 \tag{6}$$

$$I_L = \frac{1}{T}\int_0^T i_L(t)\,dt = (D - 0.5 + D_2)I_{Lpk}, \quad 0.5 < D < 1 \tag{7}$$

From Fig. 2, we can deduce the open-loop voltage gain of the 3LB converter under DCM, applying the volt–second balance principle at the period $0 < t < T$, that is, $A^+ = A^-$ $[(V_{IN} - 0.5V_O)DT = (V_O - V_{IN})D_2T]$, $B^+ = B^-$ $[V_{IN}(D - 0.5)T = (0.5V_O - V_{IN})D_2T]$. Then, we determine the corresponding D_2 for different D cases. Substituting D_2, (1) and (2), (6) and (7) into (3) yields the 3LB converter DCM voltage gain M_{VDC1-2} $(= V_O/V_{IN})$ equations with $k = R_{Load}/2Lf_s$. Solving them yields M_{VDC1-2} as shown in (8) and (9). Fig. 4 shows the plots of M_{VDC1-2} against $R_{Load}/4Lf_s$ at different D for the lossless 3LB converter. Moreover, the cross points 'X' in Fig. 4 are the simulation results obtained with Cadence, which confirm the CCM/DCM boundary (3) and (4) and M_{VDC1-2} (8) and (9)

$$M_{VDC1} = 0.5 - 0.25kD^2 + 0.5\sqrt{0.25k^2D^4 + 3kD^2 + 1}, \quad 0 < D < 0.5 \tag{8}$$

$$M_{VDC2} = 1 + \sqrt{1 + 2k(D - 0.5)^2}, \quad 0.5 < D < 1 \tag{9}$$

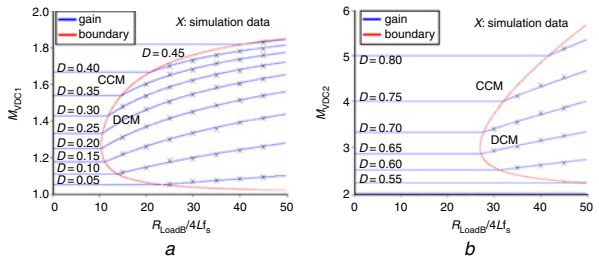

Fig. 4 *DC voltage transfer function M_{VDC1-2} against normalised load resistance at different D for lossless 3LB converter*

a M_{VDC1} against $R_{Load}/4Lf_s$, $0 < D < 0.5$
b M_{VDC2} against $R_{Load}/4Lf_s$, $0.5 < D < 1$

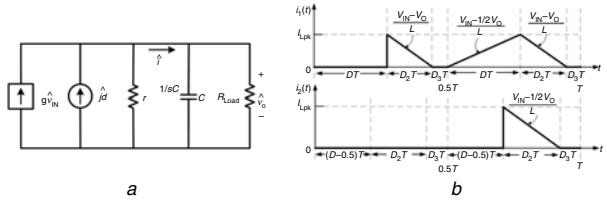

Fig. 5 *Output side small signal model of 3LB converter for DCM*

a Output side of 3LB converter DCM small signal model
b Output side current waveforms, $i_1(t)$: $0 < D < 0.5$, $i_2(t)$: $0.5 < D < 1$

DCM small signal transfer function of 3LB converter: To design its closed-loop controller under DCM, it is necessary to calculate its DCM small signal transfer function $G_{vd}(s)$. Following the same deduction method of the averaged switch network modelling from [4], $G_{vd}(s)$ is just related to the output side of the 3LB converter DCM small signal model (Fig. 5*a*). Fig. 5*b* shows the output side current waveforms with the average output side currents from (10)–(11) with the obtained D_2, where R_{e1} and R_{e2} are effective resistors of the average switch network

$$I_1 = \frac{1}{R_{e1}} \times \frac{(V_{IN}^2 - 0.5V_{IN}V_O)}{(V_O - V_{IN})}, \quad R_{e1} = \frac{2Lfs}{D^2}, \quad 0 < D < 0.5 \tag{10}$$

$$I_2 = \frac{1}{R_{e2}} \times \frac{V_{IN}^2}{(0.5V_O - V_{IN})}, \quad R_{e2} = \frac{2Lfs}{(D - 0.5)^2}, \quad 0.5 < D < 1 \tag{11}$$

By taking partial derivative of (10) and (11) with respect to V_o, D and V_{IN}, $\hat{i} = -\hat{v}_O/r + j\hat{d} + g\hat{v}_{IN}$ from Fig. 5*a*, the parameters r, j and g can be found. Finally, the 3LB converter $G_{vd}(s)$ is expressed in (12). As $\hat{v}_{IN}$ is letting = 0 for finding $G_{vd}(s)$, g can be neglected [4].

$$G_{vd}(s) = \left.\frac{\hat{v}_O(s)}{\hat{d}(s)}\right|_{\hat{v}_{IN}=0} = \frac{j(R_{Load}//r)}{1 + sC(R_{Load}//r)} \tag{12}$$

Simulation verification: The 3LB converter is built with transistor level in 65 nm CMOS process and its bode plot data are obtained by using the periodic AC analysis with Cadence Spectre simulator. With a set of design parameters $[V_{IN} = 1\ V,\ f_s = 100\ MHz,\ C_f = 15\ nF\ (r_{Cf} = 150\ m\Omega),\ C = 10\ nF\ (r_C = 100\ m\Omega),\ L = 5\ nH\ (r_L = 50\ m\Omega),\ R_{Load(D=0.3)} = 33.3\ \Omega,\ R_{Load(D=0.7)} = 65.6\ \Omega]$, Fig. 6 compares the simulated bode plots between the transfer function models (12) of boost and 3LB converters and the power stage of 3LB converter transistor-level simulation (Fig. 1). The transfer function and power stage plots of the 3LB converter are consistent for frequencies smaller than one third of f_s, which is acceptable for the closed-loop controller design. Fig. 6 clearly shows that both converters have different DCM transfer functions and characteristics, even though they have the same CCM ones.

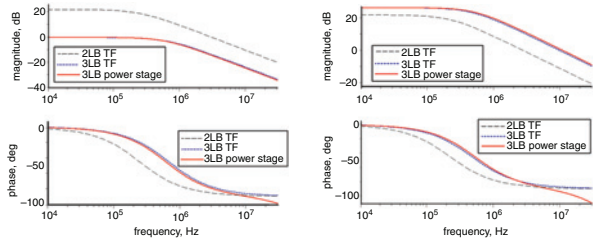

Fig. 6 *Boost converter and 3LB converter open-loop bode plot for DCM*

a When $D = 0.3$
b When $D = 0.7$

Conclusion: This Letter presents the DCM operation analysis of the 3LB converter. The DCM voltage gain and transfer function are different with the boost, even though they have the same CCM ones. This DCM operation study is important for the IC design of the DCM closed-loop controller of the 3LB converter. Finally, simulation results with MATLAB and 65 nm CMOS technology in Cadence confirm the deduced DCM theory.

Acknowledgments: This work was supported by the Macao Science and Technology Development Fund (FDCT) (SKL/AMS-VLSI/WMC/FST) and the Research Committee of University of Macau (MYRG2015-00030-AMSV and SRG2014-00007-AMSV).

Submitted: *30 September 2016* E-first: *9 January 2017*
doi: 10.1049/el.2016.3601
One or more of the Figures in this Letter are available in colour online.

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