A 27-Gb/s Time-Interleaved Duobinary Transmitter Achieving 1.44-mW/Gb/s FOM in 65-nm CMOS

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***Abstract*— A time-interleaved duobinary transmitter featuring four-way data retiming and a simplified latch + D flip-flop topology to improve the power efficiency and opening of the data eye is reported. A modified bridged shunt-peaking load using a grounded active inductor is also introduced to enhance the operational speed area efficiently. Finally, the two multiplexers, serving directly as the output driver, are summed in the current domain to avoid an extra adder. The prototype exhibits a figure-of-merit of 1.44 mW/Gb/s at 27 Gb/s, and the die area is merely 0.027 mm^2 in 65-nm CMOS.**

***Index Terms*— CMOS, duobinary, figure-of-merit (FOM), flip-flop (FF), latch, multiplexer (MUX), selector, time-interleaved.**

I. Introduction

NONRETURN to zero (NRZ) signaling [1]–[4] is widespread in microwave-speed data links, but the channel constraints, mainly brought by the 50-Ω termination and parasitic capacitance, severely limit its bandwidth (BW), especially when the data rate keeps escalating [5]. To substantially improve the data rate, signal formats that can offer a higher spectral efficiency, e.g., PAM4 [5]–[7] and duobinary [8], [9], need further investigation. Comparatively, duobinary signaling is more promising as it is simple to be demodulated in the receiver side. Yet, there are numerous subblocks [9] in the data path, such as the D flip-flop (DFF), inverter, and predriver, drawing significant amount of power. The turn-ON resistance of the passive 4-to-2 multiplexer (MUX) (pass-gate) and its previous inverter stage can also penalize the quality of the eye diagram substantially. This letter reports a time-interleaved duobinary transmitter (TI-DBTX) combining retiming and circuit-level techniques to improve the eye opening of the data eye, area, and energy efficiencies. The measured metrics compare favorably with the state-of-the-art.

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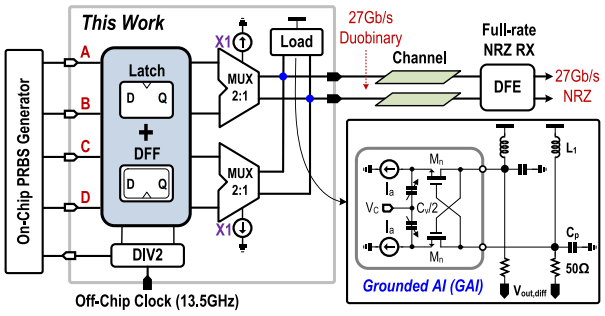


Fig. 1. System architecture of the proposed TI-DBTX.

II. TI-DBTX Architecture and Implementation

The described TI-DBTX (Fig. 1) consists of a latch + DFF array, a single-stage SUM output driver with a time-interleaved 4-to-2 MUX in the data path, and a divide-by-2 with buffers in the clock path receiving the off-chip clocks. Four independent in-phase testing data (A, B, C, D) generated from an on-chip PRBS generator are inputted to the latch + DFF array, which exploits quadrature clocking to synthesize the multiphase data. Two 2-to-1 MUXs serve directly as the final output driver under a set of quarter-rate quadrature clock. They directly convert the multiphase data to two time-interleaving data streams with 1UI phase difference in the current domain, averting the power-hungry subblocks [9] such as the inverter and the predriver before and after the MUXs, respectively. The two data streams are added at the load to output the duobinary signal. Further, the duobinary signal can be demodulated as an NRZ signal at 27 Gb/s by a full-rate NRZ receiver.

A. Serializing Using 3 Latches + 1 DFF

Our topology [Fig. 2(a)] aims at reducing the power while enhancing the eye opening of the data eye. As shown in its timing diagram [Fig. 2(b)], the upper branch is retimed by two latches, with one controlled by QP and the other controlled by IP. The transitions of the retimed data *Ad* and *Bd* are regulated to follow the rising edge of QP and IP, respectively, causing a 1UI phase difference between *Ad* and *Bd*. Meanwhile, the lower branch is retimed by QP-controlling DFF and IP-controlling latch, resulting in *Dd* leading *Cd* by 3UI. Since both data paths *B* and *D* pass through the latches controlled by IP, overall there are three different phases among the four signal paths. The four quarter-rate data holding 4UI are serialized again by a current-mode-logic MUX, with QN (IP) to control the upper (lower). In this latch + DFF array, the timing elements are simplified as 3 latches + 1 DFF, and the time delay buffer [7] between the latch + DFF array and 4-to-2 MUX is eliminated, resulting in a wider data-path BW. The multiphase clock can track the serializing operation,

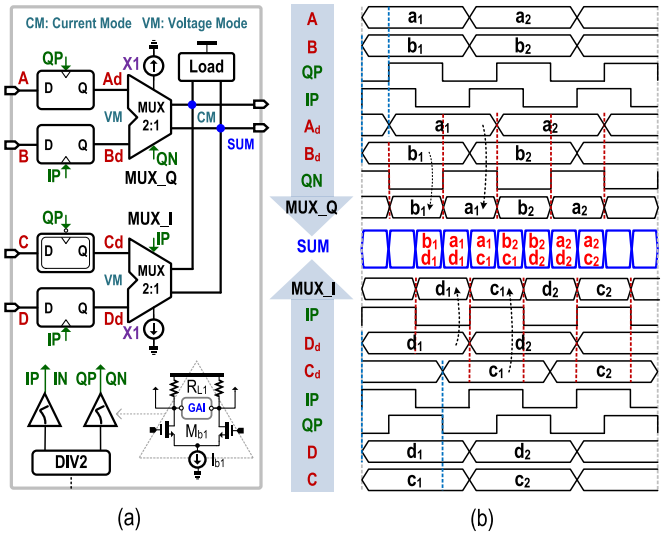
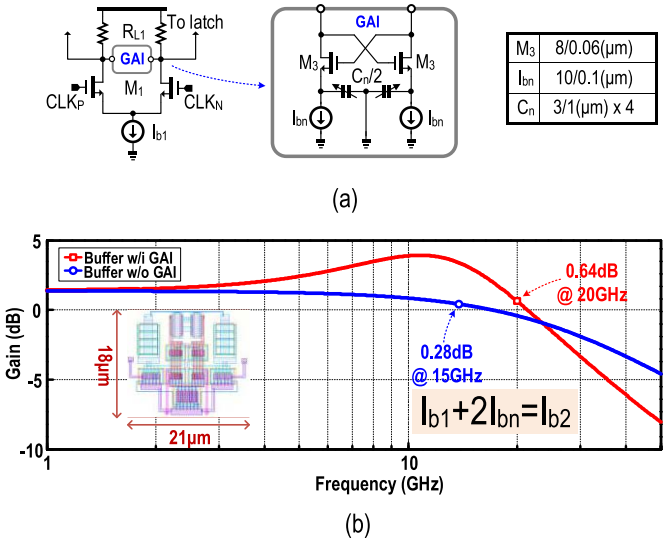


Fig. 2. (a) Implementation of the TI-DBTX and (b) its timing chart.



M_3	8/0.06(μm)
I_{bn}	10/0.1(μm)
C_n	3/1(μm) x 4

Fig. 3. (a) Swing-enhanced clock buffer using a GAI. (b) Simulated gain responses with and without GAI.

allowing the support of various data rates. Yet, the clock-to-Q delays in the latch + DFF array can limit the maximum data rate of the proposed serializing operation, and induce the data-dependent jitter at the SUM. This behavior is similar to the traditional 4-to-1 multiplexing.

B. Swing-Enhanced Clock Buffer

The proposed clock buffer [Fig. 3(a)] features a grounded active inductor (GAI) to pick up the high-frequency gain and thereby a higher output swing. The GAI is based on a positive-feedback transistorized gyrator (M_3) fixed by I_{bn} and a varactor (C_n). The simulated Q and inductance of the GAI are 1.2 and 13.2 nH, respectively. Unlike the passive inductor, the GAI occupies a very compact layout of $18 \times 21\ \mu m^2$ [inset of Fig. 3(b)]. By considering a parasitic load capacitor (C_L), the derived transfer function is

$$H(s) = A_{dc}\frac{1+\frac{s}{z_1}}{1+\frac{s}{Q\omega_0}+\frac{s^2}{\omega_0^2}} \quad (1)$$

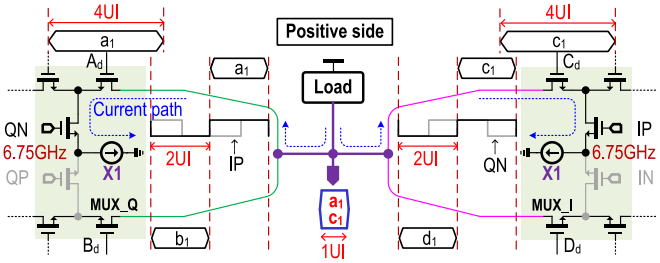


Fig. 4. Unified 4-to-2 MUX-and-SUM operation.

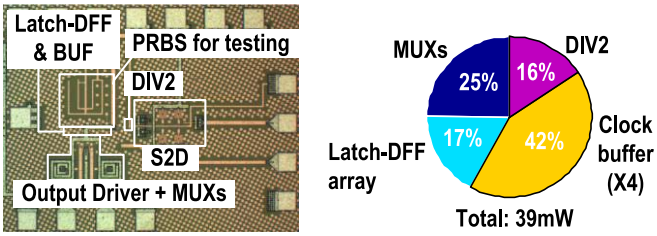
where

$$A_{dc} = g_{m1}R_{L1}, \quad z_1 = \frac{g_{m2}}{C_n}$$
$$\omega_0 = \sqrt{\frac{g_{m2}}{R_{L1}C_LC_n}}, \quad Q = \frac{\sqrt{g_{m2}R_{L1}C_LC_n}}{g_{m2}R_{L1}C_L + C_n(1-g_{m2}R_{L1})}. \quad (2)$$

The dc gain (A_{dc}) of 1.35 dB depends on the input transconductance (g_{m1}) steered by I_{b1} and the load resistor (R_{L1}), which is equal to the dc gain of the clock buffer without the GAI controlled by the tail current (I_{b2}). Under the same power budget ($I_{b1} + 2I_{bn} = I_{b2}$), the proposed clock buffer peaks the magnitude at the expected clock frequency [Fig. 3(b)], due to the occurrence of one zero (z_1) and two complex poles (ω_0 and Q), when comparing with the clock buffer without the GAI. As the clock frequency varies from 5 to 10 GHz, the time-domain output swing increases by ~1.2×, and the input–output time delay brought by the GAI is 2.7 ps, slightly >0.15 ps generated by the clock buffer without the GAI. Yet, for our targeted data rate of ~30 Gb/s such a time delay is acceptable. Comparing with a duobinary transmitter using a clock buffer without the GAI, our design shows improvements of horizontal eye opening by 0.05UI, and vertical eye opening by 10% from simulations.

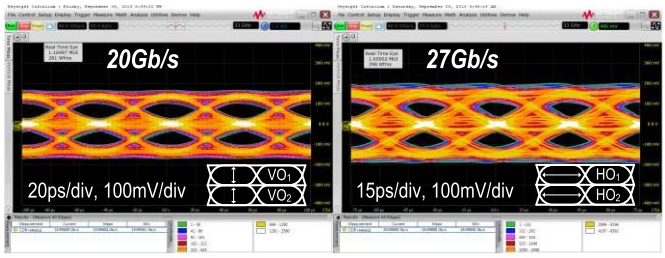
C. Unified MUX-and-SUM Output Driver

The single-stage output driver is a combination of two 2-to-1 MUXs and one adder, fully implemented with CML (Fig. 4). Since the half-rate serialization and full-rate summation are performed in the current domain simultaneously, no driver or combiner is entailed after the MUXs, which directly output the duobinary signal. Furthermore, no buffer is placed before the MUX, contrary to the buffer inserted between the MUX and the subdriver in [9], minimizing the number of subblocks in the data path. After retiming, the single-ended swing of a_1 at Ad and c_1 at Cd with a 6.75 Gb/s data rate is 400 mV_{pp}. Supposing QN and IP are with 500 mV_{pp} single-ended quadrature clock swing, voltage signals a_1 and c_1 with 13.5 Gb/s are selected by the respective MUX, which conducts the voltage-to-current conversion concurrently. These outputs in the current domain have 1/2 phase difference (1UI for the full rate). At the final output, a 27-Gb/s duobinary signal $a_1 + c_1$ will be converted back to voltage (~400 $mV_{pp,diff}$) by time interleaving. Superior to the pass-gate MUX [6], the merged MUX-and-SUM operation offers a sharper transition and a shorter delay since the clk-to-Q of the MUX has a larger clock swing [Fig. 3(a)] that can aid to mitigate the effect of serialization on the data



(a) (b)

Fig. 5. (a) Die photograph and (b) power breakdown of the fabricated TI-DBTX.



(a) (b)

Fig. 6. Measured eye diagrams at (a) 20 and (b) 27 Gb/s.

rate. As a result, the reduction of the peak-to-peak voltage due to the transmission gate is alleviated.

D. Modified Bridged-Shunt-Peaking Load

The load (Fig. 1) uses a modified bridged-shunt-peaking (L_1) and is aided by a tunable GAI (M_n and C_v) to optimize the BW of the insertion loss (S_{DD21}) and total reflection (S_{DD22}). This technique offers an auxiliary current from the GAI to drive up the parasitic capacitance at $V_{out,diff}$, generating an extra tunable zero and extending the BW of S_{DD21} up to 22 GHz. Meanwhile, a zero pair is introduced in S_{DD22}, which induces the notch at ∼15 GHz. It allows $S_{DD22} < -10$ dB within the frequency band of interest under $I_a = 0.9$ mA.

III. Experimental Results

The TI-DBTX [Fig. 5(a)] occupies 0.027 mm^2 of die area in 65-nm CMOS, and consuming 39 mW [Fig. 5(b)]. The 42% of the power is consumed in the data path, and 58% is to generate the quadrature clock to enhance the duobinary eye quality. A $2^7 - 1$ PRBS generator and a single-to-differential converter [10] are embedded on-chip for tests. The TI-DBTX was probed, and the estimated on-chip parasitic capacitance at the output is ∼80 fF. The eye diagrams were measured at both 20 [Fig. 6(a)] and 27 Gb/s [Fig. 6(b)]. At 27 Gb/s, the horizontal ($HO_{1,2}$) and vertical ($VO_{1,2}$) data eye openings are 0.53/0.53 UI and 72/74 mV, respectively, with an output swing of 389 $mV_{pp,diff}$.

Table I benchmarks this work with the prior art [6], [9]. This work succeeds in saving the power by averting several power-hungry subblocks (e.g., latch, buffer, and predriver) in the data path, and by operating the TI-DBTX in the current domain; these result in a wider data-path BW to improve the data eye and figure-of-merit (FOM). In fact, the maximum data rate of the TI-DBTX is limited by the on-chip PRBS generator.

TABLE I
Performance Summary and Comparison

Parameters	This Work	ISSCC'15 [6]	ISSCC'13 [9]
CMOS Technology	65nm	14nm	28nm
Architecture	4 : 1	4 : 1	8 : 1
Equalization	No	No	4-Tap
Driver Topology	CML with Bridged-shunt peaking + AI	SST + T-coil Peaking	CML
Modulation	Duobinary	PAM4	Duobinary
Data Rate (Gb/s)	27	40	32
TX Clock	Quarter-Rate	Quarter-Rate	Quarter-Rate
Vertical Opening (mV) between n-Level	72 / 74	61 / 61 / 61 *	20 / 20 *
Full Swing	389 $mV_{pp,diff}$	500 $mV_{pp,diff}$	500 $mV_{pp,diff}$
Horizontal Opening (UI)	0.53	0.6	0.6
Supply (V)	1.1	1.2	0.9
Power ***(mW)	39	150	97.9
Die Size (mm^2)	0.027	0.013 **	0.16
FOM (mW/Gb/s)	1.44	3.75	3.1

*Extracted values from plots ** Estimated from the die photo
***Power includes retime, divider, clock buffer and main transmitter

IV. Conclusion

This letter has proposed a TI-DBTX featuring four-way data retiming and circuit techniques in both the signal and clock paths to enhance the FOM at a small area. Fabricated in 65-nm CMOS, the 0.027-mm^2 TI-DBTX exhibits an FOM of 1.44 mW/Gb/s at 27 Gb/s compares favorably with the recent art.

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