A 120 MHZ SC 4TH-ORDER ELLIPTIC INTERPOLATION FILTER WITH ACCURATE GAIN AND OFFSET COMPENSATION FOR DIRECT DIGITAL FREQUENCY SYNTHESIZER

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Abstract *– This paper proposes an optimum design of a high frequency Switched-Capacitor IIR interpolation filter for Direct Digital Frequency Synthesizer systems. The circuit is formed by the combination of novel double sampling recursive direct-form II and non-recursive polyphase structures embedding mismatch-free analog delay lines with accurate, wideband gain- and offset-compensation achieved by Predictive Correlated-Double Sampling techniques. This filter is designed with optimized speed of the analog components in AMS 0.35 μm CMOS technology, occupies about 0.4 mm² active area and consumes about 22 mW at 3.0 V supply.*

I. INTRODUCTION

Direct Digital Frequency Synthesis (DDFS) has been increasingly employed in modern wireless communications systems, such as time division multiple access/code division multiple access (TDMA/CDMA) digital cellular systems and spread-spectrum wireless LANs, due to their fast frequency switching, high purity, reduced phase noise, and fine frequency steps when compared to conventional PLL-Based synthesis techniques [1-4]. However, the clock frequency of a conventional DDFS cell and the post-processing DAC normally requires to be raised to two or three times the Nyquist sampling rate in order to relax the complexity of the continuous-time smoothing filter which is usually implemented off-chip [2-4], as shown in Fig.1(a). Therefore, the power consumption of the synthesizer's digital section will be considerably increased. The current-steering DACs suitable for hundreds of megahertz clock rate are usually avoided due to their core-dependent transients in current switching which will produce nonharmonic spurs lying close to the sinewave frequency and which therefore cannot be filtered [4]. As a consequence, the clock frequency usually can not be raised higher enough to relax the specification of post filtering, thus still requesting an off-chip smoothing filter realization [2-4].

This paper proposes an alternative architecture by inserting a Switched-Capacitor interpolation filter between the DAC and the post filter, as shown in Fig.1(b). Here, the DDFS cell and DAC operate at the lowest sampling rate while relaxing the post analog filter to the extent that can be integrated on chip. The effectiveness of this approach results from the analog components of the SC interpolator operating at lower input sampling rate by employing efficient impulse sampled polyphase structures [5]. Thus, for instance, the images rejection of a 10-12.5 MHz bandwidth sinewave DDFS generation system, which was achieved by an off-chip analog filter [3], can be alternatively fulfilled by a 4-fold SC interpolator followed by a very simple on-chip post analog filter, hence also allowing DDFS/DAC to operate at a reduced speed. In addition, the DDFS/DAC in reference [2, 4], which produces two quadrature output sinusoids with a variable frequency in the range of 0-13 MHz, is operating at 80 MHz, and the images are attenuated by an off-chip dielectric resonator. The alternative approach is to relax the DDFS/DAC to operate at 40 MHz, and the output signal will be interpolated to 120 MHz by a SC interpolator for further decrease the complexity of the post analog filter. This paper proposes the design and implementation of such 120 MHz SC interpolator, which realizes a 4th-order Eliptic IIR transfer function with more than 60 dB image attenuation.

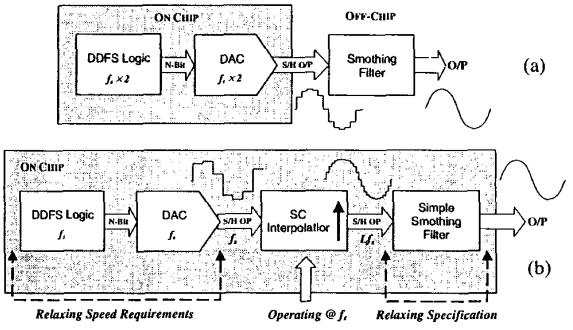

Fig.1 Conventional (a) and Proposed Alternative Structure (b) for DDFS/DAC Systems

II. DESIGN AND IMPLEMENTATION OF SC INTERPOLATOR

1. Optimized Circuit Architecture

SC interpolation filters can be implemented by employing the combination of direct-form polyphase networks and either the cascade of 1st- & 2nd-order recursive sections [6] or ladder-based recursive architectures [7]. However, the speed requirement of transconductance opamp's in both above architectures cannot take full advantage of low speed nature of polyphase structure due to their shrunk effective clock phase width, thus, in turn, narrowing the settling time of opamp's. Nevertheless, the design in this paper will employ the combination of digital-based Direct Form II recursive parts with non-recursive polyphase structures that can truly relax the opamp's to operate at lower input sampling rate [5] with respect to the maximum extended settling time.

The block diagram of the proposed 120 MHz SC 4th-order 3-fold interpolation is depicted in Fig.2. As we can see, the serial processing delay line, which is implemented by a chain of 4 active delay circuits, namely ADB's, operating at lower input sampling rate, is efficiently shared by both recursive branches and nonrecursive polyphase filters. Only one output accumulator operates at higher output sampling rate in order to be shared efficiently by each path polyphase filter, thus reducing the overall circuit complexity. Only the corresponding simplified schematic (half of the circuit) of this SC interpolation filter which is indeed implemented in fully-differential structure is shown in Fig.3 for simplicity.

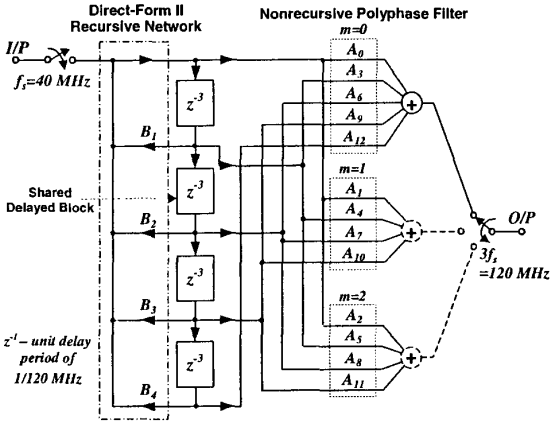

Fig.2 Digital-Based Direct-Form II Recursive and Nonrecursive DF Polyphase Structure for SC Interpolator

The Predictive-Correlated Double Sampling (P-CDS) techniques [8] are employed for accurate gain and offset compensation. The reason, first, is to avoid high-gain and very high-frequency opamp's which are the bottleneck of analog circuits, thus allowing the use of very simple single-stage low gain opamp's with a maximum exertion in their high frequency capability. Secondly, the reduction of mismatch DC offset, flicker noise and especially the nonlinearity which is very important in signal generation that must traditionally be achieved by using high-gain opamp's, will be greatly enhanced [8].

The accuracy of the delay line is the most critical part, as it will not only affect the poles and zeros of original transfer function which directly leads to the variation of passband and stopband, but also, most importantly, degrading the pole-zero cancellation owing to the multirate transformation [9,10], which will result in sharp undulations in the stopband. Consequently, not only P-CDS but also the capacitance mismatch-free techniques are employed here for constructing distortion-free analog delay line with a wideband, precise finite gain and DC offset compensation [11], as shown in Fig.3. Note that the first delay block must additionally serve as summer as well for adding the signals from recursive branches, thus this multifunction SC summer/delay circuit is realized by using Same-Sample Correction (SSC) Property [12] for achieving P-CDS. In order not to sacrifice the speed of opamp, which normally happens when using P-CDS techniques, double sampling techniques are also efficiently manipulated in recursive networks, as it will only double in a small amount SC branches which number is equal to the filter order, i.e. 4, for our design, thus maintaining the same settling time requirement of half period of lower input sampling period 12.5 ns (about 5.6 ns in [6-7] without GOC).

The last time-shared output GOC accumulator with three multiplexed summing paths for each polyphase filter also achieves high precision owing to the P-CDS technique. Note that the effect of charge coupling errors due to the error-correction capacitor C_e is normally small because the summing capacitor is much greater than it [11]. Although the opamp must operate fast with only about 4.2 ns settling time (2.7 ns in [6-7] without GOC), the required gain here and thus power are rather low (about 300 & 5.7 mW) as will be introduced next.

2. Circuit Implementation

Due to the advantage of low gain, the opamp architecture is simply the telescopic cascode input differential amplifier but with non-cascode PMOS active load, as shown in Fig.4(a). The usage of cascode transistor M_3 (or M_4) will not only eliminate the Miller effect of input transistor that will considerably reduce the bandwidth, but meanwhile enhance the gain capability, so that the gain of the op amp mainly depends on transconductance of M_1 (or M_2) and the output resistance of M_5 (or M_6). Furthermore, the output swing is also enlarged due to allowance of single PMOS active load when compared to typical telescopic opamp. The control of the output common-mode voltage is provided by a dynamic SC common-mode feedback circuit which will drive the gate of M_{7a} only, instead of both M_{7a} and M_{7b} to reduce the effect of charge injection and clock feedthrough. The faster opamp in the output accumulator achieves 933 MHz open-loop unit-gain frequency and 51 dB gain and 58° phase margin for a capacitive load of 2.4 pF, as shown in the HSPICE-simulated frequency response of Fig.4(b). Simulations show a 0.1% settling time of about 3.2 ns for a 1Vpp output step with 3.1 pF sampling capacitor, 2.2 pF feedback capacitor and 1 pF loading capacitor. The power consumption is as lower as 5.7 mW for 3 V supply. The largest transistor is the input differential pair M_1 and M_2 with the width of 550 μm. The slower opamp used in active delay line exhibits 451 MHz unit-gain frequency, 51 dB gain and 68° phase margin for 4 pF loading. The simulated 0.1% settling time is 11.4 ns (2.4 pF, 0.8 pF and 3 pF) with a power of 4 mW.

In order to reduce the signal-dependent charge injection and clock feedthrough which is quite serious in such high frequency operation, the fully-differential (FD) combining clock advanced techniques [13] are used here for turning off all the switches near the virtual ground node of opamp first (For simplicity, not shown in Fig.3). Simulation results show that the single NMOS switch has smaller fully-differential clock feedthrough effect than CMOS switches although the signal-independent offset is slightly larger, which has no effect in FD circuit. So, only NMOS switches are used in this circuit. This is possible because the common-mode voltage here is set to 1.1V due to the required maximum differential output of only 2Vp-p, being the nonlinearity of the resistance of CMOS and NMOS switches similar within (0.6-1.6 V) for 3 V supply. This will not only relax the circuit complexity but simplify

the required clock phases. Besides, dummy switches are also used together with the circuit output sampling switches. Switch sizing is ranged from width of 3.5 μm to 35 μm to accommodate the different loading conditions.

The overall filter contains 376 of 100 fF unit capacitance being the maximum spread 21.6. In fact, the overall capacitance area and spread have already been efficiently saved about 40% and 50% respectively due to the optimum scaling with the manipulation of two parasitic-compensated toggle SC branches in A^e_0 and A^e_{11}, as shown in Fig.3. Hence, the overall circuit realized in 0.35 μm CMOS consumes only an active chip area of about 0.4 mm^2 and a total DC power around 22 mW (not including the clock generation).

The simulated amplitude response of this SC interpolator is illustrated in Fig.5 with also the comparison to the ideal and uncompensated one. The simulations are preformed by using switches with on-resistance, and opamp gain of 300, and especially a large input parasitics of 0.5 pF presented at the opamp input which will considerably degrade the SC circuit performance. As we can see, all the unwanted image bands located at 27-40 MHz, 40-53 MHz, 67-80 MHz and 80-93 MHz have been attenuated with minimum 60 dB to achieve nearly 10 bit accuracy which is usually enough for DDFS systems. It is clearly evident that the variation of the pole and zero placement due to the finite gain error and parasitics in our design is very small, and thus amplitude response is almost fully matched to the ideal one. Especially, when comparing to the uncompensated circuit with high gain of 5000, the proposed circuit has the equivalent passband but with much smaller stopband deviation. While for the uncompensated one with gain of 300, its passband and especially stopband varies more than 1.6 dB and 20 dB respectively due to the large distortion of the placement of poles and zeros.

III. Conclusions

An optimized design and implementation of a 4th-order elliptic SC interpolation filter with the sampling rate increase from 40 MHz to 120 MHz have been proposed for relaxing speed of both digital DDFS cell and DAC as well as complexity of post analog filter, thus leading to the possibility of integrating the simple post filter on chip. The operating speed of almost all opamp's in circuit has been reduced to the lower input sampling rate by using the efficient digital-based recursive polyphase structures with partial double sampling. Moreover, predictive-correlated-double sampling techniques have also been employed for achieving the accurate, wideband gain and offset compensation, thus allowing very simple low-gain opamp which has been implemented with 933 MHz bandwidth and power of only 5.7 mW. The overall circuit will require about 0.4 mm^2 active chip area with total DC power consumption of around 22 mW for 3 V supply in 0.35 μm CMOS, and the overall responses achieve a good agreement to the ideal theoretical expectation.

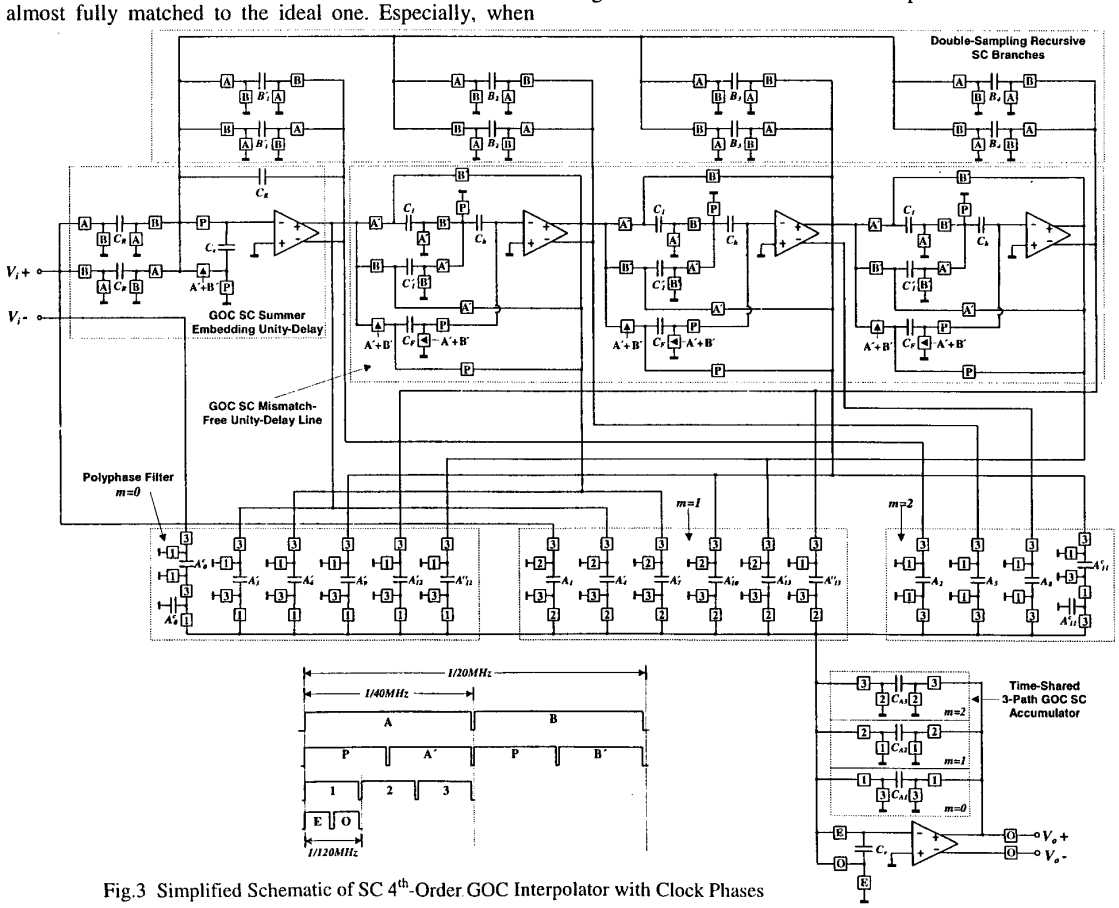

Fig.3 Simplified Schematic of SC 4th-Order GOC Interpolator with Clock Phases

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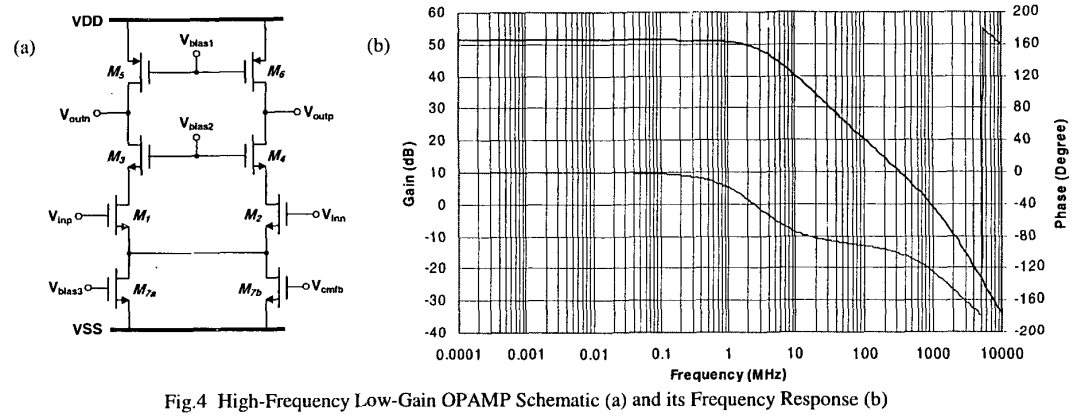

Fig.4 High-Frequency Low-Gain OPAMP Schematic (a) and its Frequency Response (b)

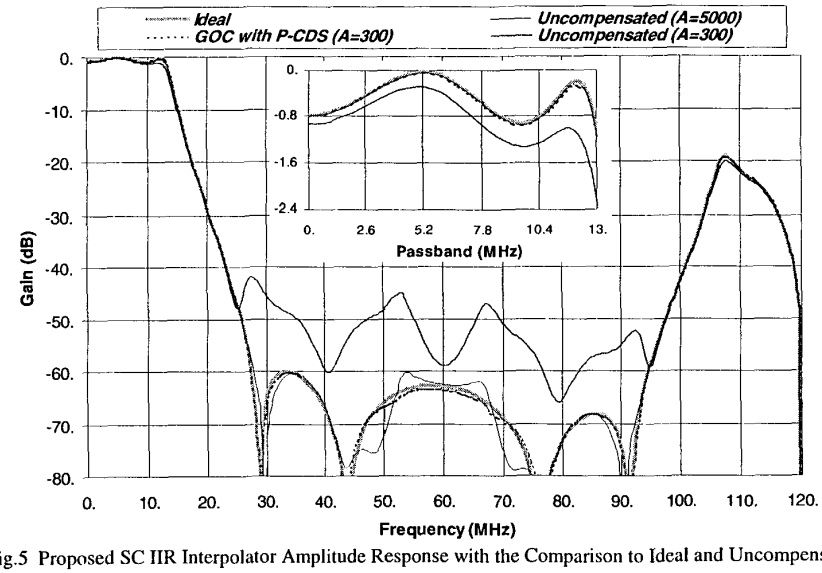

Fig.5 Proposed SC IIR Interpolator Amplitude Response with the Comparison to Ideal and Uncompensated One