A HIGH-SPEED FREQUENCY UP-TRANSLATED SC BANDPASS FILTER WITH AUTO-ZEROING FOR DDFS SYSTEMS

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ABSTRACT

This paper presents the design and implementation of a 160 Msample/s output, offset-compensated, linear-phase, frequency up-translated Switched-Capacitor bandpass filter with 28.5 MHz midband frequency for a DDFS system. This bandpass system translates the 40 Msample/s, 11-12 MHz bandwidth signals from DDFS output to a higher 160 Msample/s, 28-29 MHz outputs with a 40 dB rejection of the unwanted frequency-translated signal bands. Special considerations and design in both circuit architectures and layout arrangements for dealing with non-ideal properties in realization of the high-speed analog and digital clock circuits will be discussed in terms of the speed relaxation, noise and mismatching reduction. The system is designed with 0.35 μm CMOS technology and verified by behavioral, transistor-level and layout-extracted simulations. The active layout area occupies about 1.3 mm × 2.7 mm and the circuit consumes about 138 mW for analog and 32 mW for digital at 3.0 V supply.

1. INTRODUCTION

Frequency-translated sampled-data filtering were initially introduced for very narrow band filtering [1]. Their usage has since then been extended to many more applications; the subsampling architecture with sampled-data filtering which combines both functions of channel selection and frequency downconversion for radio wireless receiver is one of the notable examples nowadays [2, 3]. This paper presents a complementary approach combining both frequency-band selection with frequency upconversion for using in the Direct Digital Frequency Synthesis (DDFS) system which has been increasingly employed in modern wireless communications systems due to their fast frequency switching, high purity, reduced phase noise, and fine frequency steps when compared to conventional PLL-Based synthesis techniques. This alternative DDFS system employs an optimum-architecture Switched-Capacitor (SC) frequency up-translated bandpass interpolation filter which allows the Operational Transconductance Amplifiers (OTA's) to operate at lower DDFS clock rate, hence achieving several fold speed reduction in the core DDFS logic and DAC as well as a relaxation of the specifications of the post analog smoothing filter. In this paper, a 160 Msample/s output SC bandpass filter (BPF) is described for up-translating 1 MHz bandwidth signal at 11-12 MHz to higher 28-29 MHz with a 4-fold sampling rate increase from DDFS system clock 40 MHz.

Detailed design and implementation in 0.35 μm CMOS, based on multirate polyphase-based interpolation structure with auto-zeroing techniques for reducing the speed requirement of amplifiers and enhancing the signal purity, will be described with the consideration and special treatment to inherent non-ideal imperfections of analog integrated circuits. Both transistor and layout-extracted simulation results will be provided for verifying the circuit effectiveness.

2. FREQUENCY UP-TRANSLATED FILTERING FOR DDFS

The combined architecture of DDFS system and frequency up-translated SC bandpass filtering and its corresponding frequency spectrum are presented in Fig.1. The mid frequency of DDFS output signal baseband is f_0 and its frequency imaging bands appear around the multiples of DDFS/DAC clock rate f_s, i.e. $nf_s \pm f_0$, the frequency up-translation is achieved by selecting the wanted frequency band and rejecting the remaining unwanted ones through the bandpass filtering with together a sampling rate increase, thus such filtering is also called frequency up-translated bandpass interpolation. The output frequency up-translated signals can be further smoothed by either a simple lowpass or bandpass analog filter. It is worth to point out that, different from frequency down-translation, due to the sampled-and-held nature of the signal at the output of DDFS/DAC, different gain errors will be introduced over each frequency band according to sin x/x shaping at DDFS/DAC clock rate. Therefore, in addition to the frequency band selection and sampling rate increase, the SC BPF needs also to have an extra functionality to compensate those gain errors. This can be achieved by the recently proposed improved multirate polyphase-based interpolation structures, which will recover such sin x/x shaping gain errors over the entire frequency axis [4], consequently allowing an extra degree of freedom for designers to assign both the passband and stopband frequency, as well as the required level of attenuation.

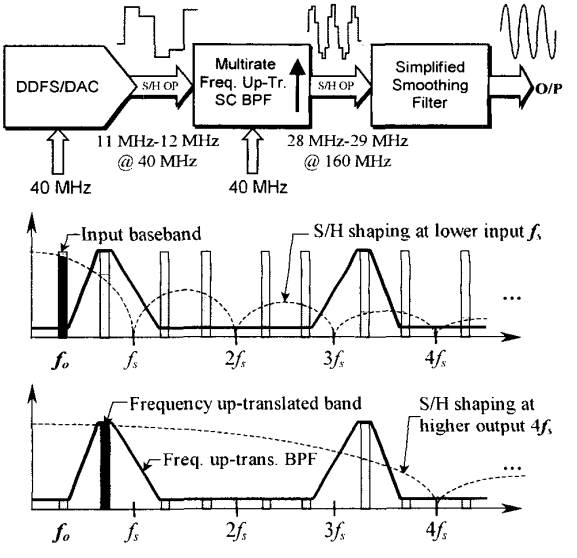

Fig.1 Frequency up-translated bandpass filtering for DDFS systems

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In this application, the DDFS system generates the 11-12 MHz output signals at the clock rate of 40 MHz, the SC bandpass filter selects the 1st (n=1) lower sideband of the images with a 4-fold increase of sampling rate to 160 MHz, a passband ripple smaller than 0.8 dB and the unwanted image band rejection around 40 dB. Especially, in order not to degrade the signal purity, the system is also required to alleviate the frequency-translated image components of the DC offset associated with DDFS/DAC output folded at the lower 40 MHz clock rate and its multiples, especially the one located near the passband which won't have enough attenuation.

3. FILTER IMPLEMENTATIONS

3.1 Filter Architecture

The multinotch 15-tap FIR filtering is employed here due to its low passband sensitivity and the narrower signal band nature. The non-recursive Active-Delay Block (ADB) polyphase-based SC interpolation structure [4] is suitable and employed for this FIR filtering whose block diagram is shown in the Fig.2. The core of the filter is composed by a mixed serial-parallel ADB delay line and 4 parallel polyphase filters. The superiority of this ADB polyphase interpolation structure is explicit by the fact that both ADB delay line and polyphase filter bands, which are the most critical area & power consuming parts of the whole circuit, operate at lower input sampling rate. However, the non-ideal effects like the errors caused by offset and finite gain and bandwidth of the OTA's will be propagated and accumulated through the serial delay line and 4 path polyphase filters. Especially, the offset errors generate the pattern noise spurs at lower sampling rate 40 MHz and its multiples, and the Monte-Carlo simulations show that the ±6 mV ranged offset can impose noise spurs above –40 dB level which seriously degrade the signal to noise ratio. Therefore, auto-zeroing technique [5] is employed to compensate the offset effects. Note that the increased demand for slew rate in auto-zeroing SC circuits due to the reset nature is valid for high oversampling-mode processing, while the slew rate is even being relaxed relatively in this frequency-translated filter due to the low oversampling ratio at input, e.g. OSR=1.67. In addition, the mixed serial-parallel delay line configuration is designed for achieving maximum required delay but with minimized accumulated errors. The input S/H stage is designed mainly for testing purpose, as it is not mandatory if the filter clock synchronizes with DDFS/DAC clock and also the DDFS/DAC has enough buffering capability.

3.2 Auto-zeroing SC Delay Circuit and Polyphase Filter

For simplicity, only the simplified clock phases and positive parts of a z^{-6} auto-zeroing SC delay circuit and SC polyphase filter 0 are presented in Fig.3(a) and (b), respectively, as the circuit is implemented in fully-differential structure.

The charge-transferring-free property of the delay circuit eliminates the capacitance ratio mismatch errors, alleviates the finite gain errors and also enhances the achievable speed. Note that the extra switches *sw1* & *sw2* are mandatory for breaking the resistive paths during the charge-holding phase of SC branch *1* and *2*, thus eliminating the signal-dependent clock-feedthrough and charge-injection errors. Since both the slew rate and feedback factor of the close-loop delay circuit are proportional to the capacitance value of sampling and holding capacitor, a compromised value is found at 0.48 pF.

The FIR filter tap weights are implemented by direct capacitance ratio of SC branch to the summing capacitor, as shown in Fig.3(b), so the positive and negative coefficients are achieved by either in-phase direct charge coupling or out-phase charge transferring from either positive or negative outputs of delay circuit depending on their required delay and the availability of the outputs of delay circuit (as there is one reset phase). The maximum capacitor spread is 8 and the unit capacitance has been assigned as 100 fF and 150 fF for polyphase filter 0, 2 and 1, 3, respectively, according to the different equivalent capacitance loading.

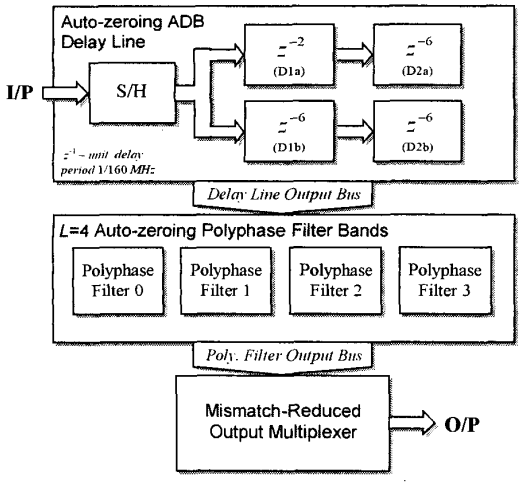

Fig.2 System architecture of the frequency up-translated SC BPF

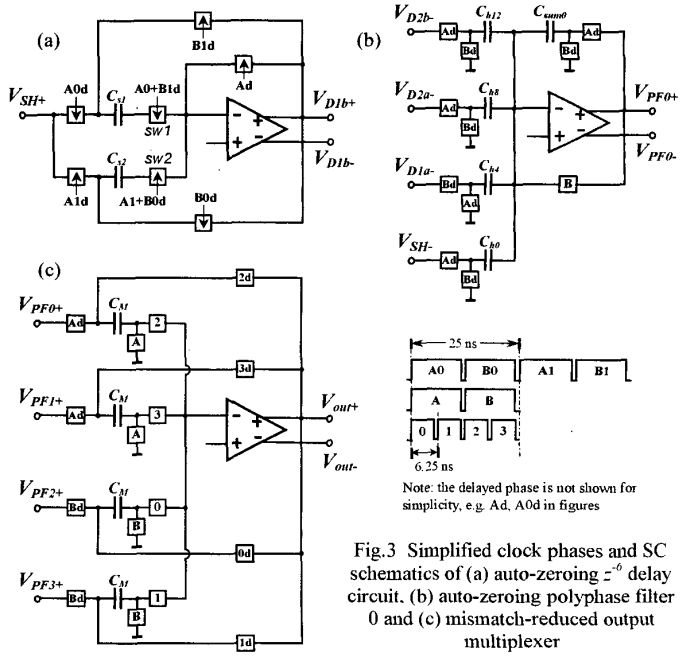

Fig.3 Simplified clock phases and SC schematics of (a) auto-zeroing z^{-6} delay circuit, (b) auto-zeroing polyphase filter 0 and (c) mismatch-reduced output multiplexer

The OTA in the delay and polyphase filter is implemented in single-stage telescopic-cascode structure. The layout-extracted SpectreS simulations show that the OTA achieves 686 MHz (typical mean) open-loop unit-gain frequency, 70 dB gain and 57° phase margin for 4 pF capacitive loading. The OTA has about 0.1% settling time of 7.8 ns and 0.57 V/ns slew rate for a 1Vp-p output step with 3 pF sampling, 1 pF feedback and 3 pF loading capacitors. The power is 12.8 mW for 3 V supply including wide-swing cascode biasing circuitry. The input and output common mode levels are all set to 1.15 V for the required reset operation in auto-zeroing technique.

3.3 Mismatch-Reduced Output Multiplexer

The output multiplexer stage shown in Fig.3(c) is also implemented for interfacing the post smoothing filter. Although it needs to multiplex 4 polyphase filter outputs at 160 MHz sampling rate, due to the efficient configuration of charge-transferring free and full output sampling period (6.25 ns) operations, the achievable speed of this multiplexer has been maximally enhanced, and the finite gain and offset errors of OTA mainly contribute to a net gain shift and DC offset of the circuit. The elimination of charge-transferring leads to a significant reduction in the 4 path gain mismatching, which will lead to mirror sidebands exactly overlapping onto the unwanted image bands that cannot be removed from SC BPF. Note that the mismatching among 4-path sampling and holding capacitor value still renders the speed mismatching of 4 paths, which, however, can be neglected, e.g. 5% capacitor value mismatch results mirror image sidebands always below -60 dB. The double-sampling SC CMFB circuit is used in multiplexer mainly for increasing the matching among the 4 paths. Besides, to alleviate the increased non-linear harmonic distortion caused by the slewing in the output waveform, due to the lower oversampling ratio, the speed of multiplexer OTA is specially raised. As this is the sole fast OTA in the circuit, the extra power is not significant when compared to the overall power.

From the layout-extracted simulation results, the OTA exhibits 900 MHz unit-gain frequency, 66 dB gain and 54° phase margin for 4 pF loading and consumes about 22 mW. The whole SC multiplexer takes about 2.3 ns to settle at 1 V voltage step input with an initial 1.3 V/ns slew rate from the layout-extracted simulations.

3.4 Low Phase-Offset Multi-Phase Generation

To reduce the signal-dependent clock-feedthrough and charge-injection errors, the clock-delayed technique is used, and therefore, totally 21 phases (no need for complementary phases, as only NMOS switches are used due to the low common-mode voltage) are required to be generated from one master 160 MHz clock input. However, not only the substantial delay mismatches from standard frequency divider and non-overlapping clock generation circuit but also unbalanced digital power supply noise will introduce large timing errors or fixed offset among time-interleave phases which will render an unbalanced duty-cycle sampling. Such error, which is equivalent to a periodic non-uniformly sampling, imposes the mirror sidebands around multiples of the lower sampling frequency and the sideband magnitudes depending on the actual sampling phase offsets and the signal frequency [6]. Different from downsampling, such sampling errors are generated at the high-speed output stage for frequency up-sampling and thus the resulting sidebands will overlap onto the rejected image bands, similar to the path mismatches, that cannot be removed by the interpolation filter, while they will fold within the stopband before the filtering stage in downsampling case. This problem becomes very serious especially for high speed. To ensure the overall unwanted image band having below 40 dB loss, the fixed phase offset must be smaller than 40 ps among interleave phases 0, 1, 2 and 3 when counting also the capacitance ratio mismatches. Thus, dual approaches have been designed to minimize this jitter error [6]: first, all phases will be generated by equal-delayed digital logics based on two 50 % duty-cycle phases ideally provided by a specific frequency divider (÷2) and non-overlapping clock generation circuits; second, to minimize the mismatches imposed from the logic gates passed by 8 phases for multiplexer, a special edge-triggered circuit is also proposed to trigger their rising edges from one same phase, so that the mismatches will only happen in the buffer circuits. The dynamic power, mainly dominated by the clock buffers, is about 32 mW (rms) in which 22 mW for the low-speed clock generation and 10 mW for the high-speed multiplexer.

4. LAYOUT AND EXTRACTED SIMULATION RESULTS

The circuit layout (not including PADs) in 0.35 μm double-poly triple-metal CMOS with lightly-doped substrate is shown in Fig.4 with the active core area about 1.3 mm × 2.7 mm. Special cares have been taken for the symmetry in not only analog but also digital interleave clock circuits for reducing the mismatches. Analog and digital supplies are separated and all decoupled on chip to a same shared ground which bias the whole chip substrate with ample substrate contacts. Simulation shows that it helps to reduce the power supply noise when compared to the use of separate on-chip analog and digital grounds. This is mainly because that all signals inside the chip will now refer to the same ground voltage level even if it is noisy, and during the signal transferring between different supply domains, which is the most current-spike-consumed part of SC filters, the return currents will be flowed inside the chip rather than through the inductive package. It is also worth to point out that two separate supplies are used for digital clock generation: one to the clock generation for low-speed delay line and polyphase filters which will drive large current spike periodically during the phase 0 & 1 and phase 2 & 3 (2 times of the output sampling period), and another to that for the high-speed output multiplexer which is very sensitive to the phase offset errors. This is exceptionally important especially for multirate SC circuits, as this makes the same current drawing or indeed the same decoupled supply voltage variation in each phase 0, 1, 2 and 3 period, thus rendering a decreased phase offset error. From simulations, it aids to reduce the phase offset of at least 100 ps, when compared to the use of one shared supply.

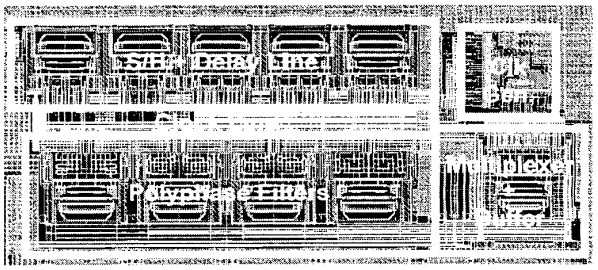

Fig.4 Layout of the frequency up-translated SC BPF

Shielding by lower layer or N-well is widely used in the layout for either sensitive analog signal or noisy digital clock lines. Especially, shielding the long noisy clock phase distribution lines by metal 1 connected to digital supply Vdd gets further 20% reduction from simulations in power supply noise when compared to shielding to ground, as this minimizes the maximum peak current loop drawn

from the clock line parasitics happening at the rising edges of clocks where the original phases and their delayed version are raised at the same time. Wide-sheet power supply lines are used for minimizing the voltage drops across these lines and MOSFET capacitor are filled in any unused space for obtaining enough decoupling capacitance from the supplies to ground, and the capacitance values are more than 100 pF so that the power supply noise can be controlled within 200 mV in the worst case simulations.

The circuit is verified with behavioral, transistor-level and layout-extracted simulations. Fig.5 shows the Monte-Carlo amplitude response simulation with respect to all capacitance ratios, which are independent zero-mean Gaussian random variables with the deviation within 2.1 % (or σ_e=0.7 %), showing that the worst and average case of the images stopband is below -40 and -50 dB, respectively.

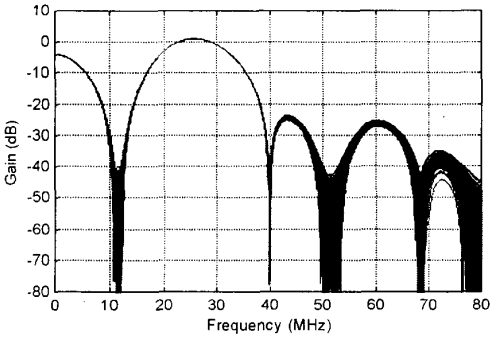

Fig.5 Monte-Carlo amplitude response simulations (σ_e = 0.7 %)

Fig.6 presents the frequency spectrum of up-translated 29 MHz output from SC BPF with the 11 MHz, 1.5Vp-p sinusoidal input. This result is obtained from FFT of the worst-case speed & temperature transistor-level transient simulation with the capacitance ratio value from the random mismatches within 2.1 % and OTA differential pair transistor size from mismatches at maximum 10 % plus also the simplified inductive package model. As we can see, the input baseband signal at 11 MHz and its images at 51 MHz, 69 MHz have been attenuated about 40dB, all the other tones are the frequency translated-images of the harmonics sampling at lower input and higher output sampling rate and their multiples, and their total harmonic distortion is calculated about 50dB below the signal. The worst harmonic tone with –54 dB located at 73 MHz is the addition of the 3rd-harmonic of signal 11 MHz from low-speed filter core sampled at 40 MHz and 3rd-hamonic of the output 29 MHz from the output multiplexer sampled at 160 MHz.

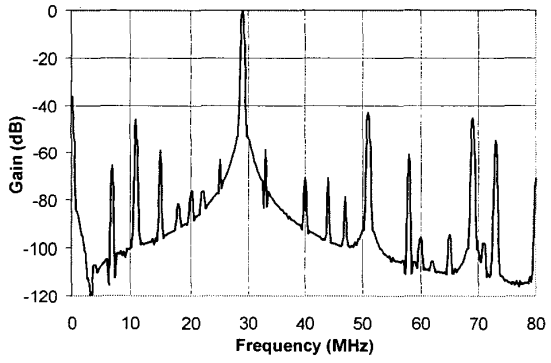

Fig.6 Spectrum of 29 MHz output signal with 1.5Vp-p 11 MHz sinusoidal input from the worst-case transistor-level simulation

Fig.7 is the impulse transient response of the circuit obtained from the layout-extracted simulation with the simplified package model under the worst-case speed and temperature. It shows clearly the achieved 15-tap symmetrical impulse response of the FIR BPF.

5. CONCLUSIONS

The design and implementation of a novel frequency up-translated, 40 Msample/s input, 160 Msample/s output, 28.5 MHz midband frequency SC bandpass filter for DDFS systems has been proposed in the paper for upconverting 11-12 MHz input signals to 28-29 MHz signal outputs. Multirate FIR polyphase-based parallelism, auto-zeroing techniques and low phase-offset jitter clock generation as well as special layout arrangement have been employed in the system for achieving high-speed, lower-power operation without degrading the original signal purity. Both behavioral, transistor-level and layout-extracted simulations have been performed for verifying the effectiveness of the proposed circuit techniques. The whole system consumes about 1.3 mm × 2.7 mm active layout area and 138 mW analog static power (including input S/H stage) and 32 mW digital power at 3.0 V supply.

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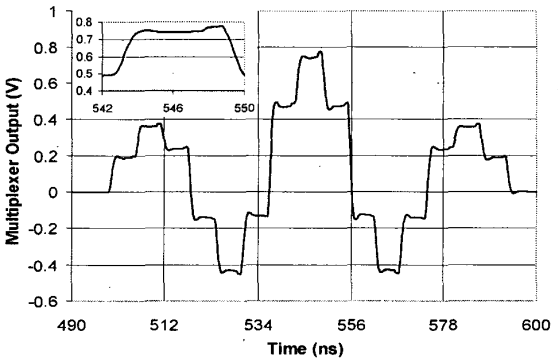

Fig.7 Impulse transient response from layout-extracted worst-case simulation

MMIC ACTIVE FLOATING GYRATOR DESIGN AND ACCURATE MODELLING

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ABSTRACT

This paper introduces a novel floating gyrator circuit. The circuit is based on two differential pair stages used as voltage controlled current sources (VCCS). In order to characterize the component, an accurate passive model is extracted by means of a technique based on symbolic analysis. A prototype has been designed using the Philips ED02AH PHEMT foundry process to validate the proposed model.

1. INTRODUCTION

The synthesis of microwave monolithic integrated circuit (MMIC) filters constitutes an important issue in today telecommunication applications and in particular their monolithic implementation is very suitable in order to reduce cost and dimensions for a majority of communication devices.

One of the difficulties commonly encountered in the MMIC filter design is the lack of inductors with acceptable quality factors especially in a floating configuration. Many authors have intensively worked upon floating gyrator implementation in MMIC technology [1–8].

The use of active inductors requires an accurate modeling of the component behavior. It is very important to predict how the active inductor deviates from the ideal characteristics in order to quantify loss mechanisms, parasitic capacitors and even to calculate the effective inductance value. Commonly, undesired effects are simply evaluated using an equivalent resistance in series to the real inductor. The resulting equivalent inductance is thus evaluated dividing the reactance by the angular frequency, leading to unacceptable results such as inductance value increasing with frequency.

The paper mainly deals with a new floating active inductor topology and its modelling. Although the proposed model extraction is tested on a novel topology, the procedure is quite general and is based on the maximum testability property of a suitable passive model. By considering such model as a linear circuit, analog circuit fault location procedures can be applied. In fact the extraction procedure has been developed by considering its similarity with the solvability problem of the fault diagnosis equations written in a symbolic form: in both cases the circuit component values must be determined starting from the measurements. In order to obtain this, the testability and ambiguity group concepts, which have been introduced before in the fault diagnosis of linear analog circuit [9-11], are of primary importance. Testability gives the maximum number of circuit components which can be theoretically determined starting from the network function information, i.e. circuit measurements. An ambiguity group is a set of components whose variations produce the same measurement values. Hence it is impossible to uniquely determine values of components which belong to an ambiguity group. In other words the lumped model parameters must belong to the optimum set of testable components. The optimum set is a set of components representing all the circuit elements and giving unique solution for the extraction problem since the components do not belong to any ambiguity group [10]. This information is given by the analysis of the network parameter matrix, written in a symbolic form. The paper is summarized as follows: in Section 2 the novel floating gyrator circuit is introduced and a passive lumped model is proposed. In Section 3 a procedure based on symbolic technique is described, in order to validate the passive model. Finally in Section 4 the behavior of the MMIC prototype is reported, discussed and compared with the extracted model.

2. THE MMIC GYRATOR

2.1 Basic principle description

The gyrator principle could be easily understood as the act of exchanging voltage and current with each other at the terminals of a two-terminal device. Thus, we first use a VCCS to obtain a current proportional to the input voltage, flowing in the impedance Z_0 (Fig. 1). Then we add another VCCS to generate a current proportional to the voltage raised across Z_0 at the input terminal.

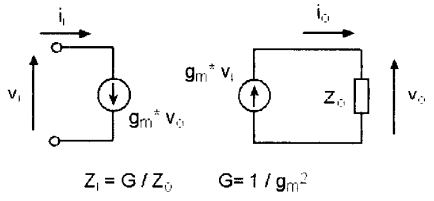

Figure 1. Gyrator working principle.

To realize these simple ideal configuration two differential stages are used (Fig. 2). In spite of the increased complexity this configuration very closely matches the ideal behavior of the scheme in Fig.1. Furthermore the gyration factor is quadruplicated with respect to Fig.1 because the control voltage drawn at the load and at the input terminals are halved.

Fig.3 shows the full differential component implemented by using the Philips ED02AH PHEMT foundry process. Although the circuit topology is better implementable in CMOS technology a state of the art technology is used in order to demonstrate the high

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