# HIGHLY ACCURATE MISMATCH-FREE SC DELAY CIRCUITS WITH REDUCED FINITE GAIN AND OFFSET SENSITIVITY

**Seng-Pan U [1], R.P.Martins [1'], J.E.Franca [2]**

1 - University of Macau, Faculty of Science and Technology, P.O.Box 3001, Macau, E-mail - fstspu@umac.mo
(1' - on leave from IST/Portugal, E-mail - rtorpm@umac.mo)

2 - Instituto Superior Técnico, Integrated Circuits and Systems Group, Av. Rovisco Pais, 1, 1096 Lisboa Codex, Portugal, E-mail - franca@gcsi.ist.utl.pt

**ABSTRACT –** Novel Switched-Capacitor (SC) delay circuit architectures, all insensitive to capacitance ratio mismatch, non-ideal amplifier's DC offset and $1/f$ noise with also either narrow or wideband compensation of finite gain error, will be proposed in this paper. A rigorous comparison of the different structures with respect to magnitude, phase and offset errors will be presented for illustrating their effectiveness. Finally, a flexible implementation of arbitrarily longer delay by the proposed circuits will be further developed in some design examples of unit and double unit delay circuits with only one amplifier and unchanged accuracy performance.

## 1. INTRODUCTION

Switched-Capacitor (SC) delay circuits, as the basic building block of SC circuits, can be applied in widespread sampled-data signal processing areas, such as sample-and-hold interface specialized multirate SC decimators and interpolators, and especially in FIR filtering circuitry [1-7]. The elimination of non-ideal properties such as amplifier DC offset and finite gain errors as well as physical capacitor mismatch of SC circuits becomes more and more necessary when the accuracy demand in applications is ever growing, especially when the supply voltage needs to be reduced [8-14]. However, SC delay circuits that fully meet all these requirements have not yet been proposed or implemented [1-5]. This paper will present different and novel SC circuit structures, which fulfill all the above demands with either narrow band or wideband compensation. A rigorous theoretical analysis and computer simulation will elaborate the performance of those structures. Finally, this paper will also propose flexible and efficient building blocks that can realize unit or even longer delays without increasing amplifier number, thus allowing the implementation of high performance Gain-, Offset Compensated (GOC) delay lines with a minimized number of stages.

## 2. CIRCUIT ARCHITECTURES

In order to allow the comparison with the novel GOC structures presented next, a typical uncompensated SC delay circuit is depicted in Fig.1(a). Based on this assumption, we propose here several distinct implementations of GOC and mismatch-free SC delay circuits in Fig.1(b) – (g) that include different arrangements of storage and cancellation of the nonzero virtual ground voltage for realizing Correlated Double Sampling - CDS, [14]. It is also evident that the input sampled and the output signals of all these circuits are represented by the same charges on the same capacitor, which implies that no charge transferring operation exists, thus eliminating physical mismatch problem of capacitance ratio.

The novel circuits proposed in Fig.1(b) and Fig.1(c) are obtained by modifying the original GOC integrators presented in [8] and [10] respectively to achieve the mismatch-free property. These circuits realize the conventional CDS using feedback path of $C_F$ which has stored previous phase output voltage for generating the nonzero inverting node voltage and for approximating the current phase gain error that will be canceled in the next output phase. The only disadvantage occurs when the input is not over-sampled (meaning that the output varies much from one phase to the next), the finite gain effect will be increased extensively which implies a frequency-dependent compensation. Especially, the sampling-signal capacitor $C_1$ of the circuit in Fig.1(b) will couple certain amount of charges to $C_F$ depending on the variation of input signals between two phases, thus affecting the inverting node voltage. By having a fixed charge redistribution between the offset-storage capacitor $C_h$ and $C_F$, the circuit in Fig.1(c) will have a better performance in frequency-dependence behavior.

The circuit of Fig.1(d) corresponds to our new mismatch-free version of the gain stage presented in [9] and Fig.1(e) to a simplified version of the unity-gain buffer circuit in [11]. They are indeed a further enhancement of the circuits of Fig.1(b) and (c) respectively with anticipatory compensation scheme (Predictive CDS) which predicts a much closer approximation of finite gain and offset errors. These errors are expected to be presented in next output phase by performing a similar switching operation preliminarily, thus attaining a very accurate and almost frequency-independent compensation. However, these two circuits require an extra phase for coupling them with other stages due to the fact that the input must be held constant over two phases.

The above mentioned input S/H condition no longer exists in the final two circuits of Fig.1(f) and Fig.1(g) that perform similar precision but with extra phases. We employ the same circuit configuration of Fig.1(c) to achieve the anticipatory compensation successively with multiple phases, as shown in Fig.1(f). Without degrading the speed of the amplifier, this is especially appropriate for sampling rate converter circuits due to their multirate nature, thus. Lastly, we have also implemented the anticipatory compensation delay circuit of Fig.1(g) with the same sample correction property as referred in [13] by switching the virtual ground from un-compensated to error-compensated in the same output phase.

0-7803-5471-0/99/$10.00©1999 IEEE

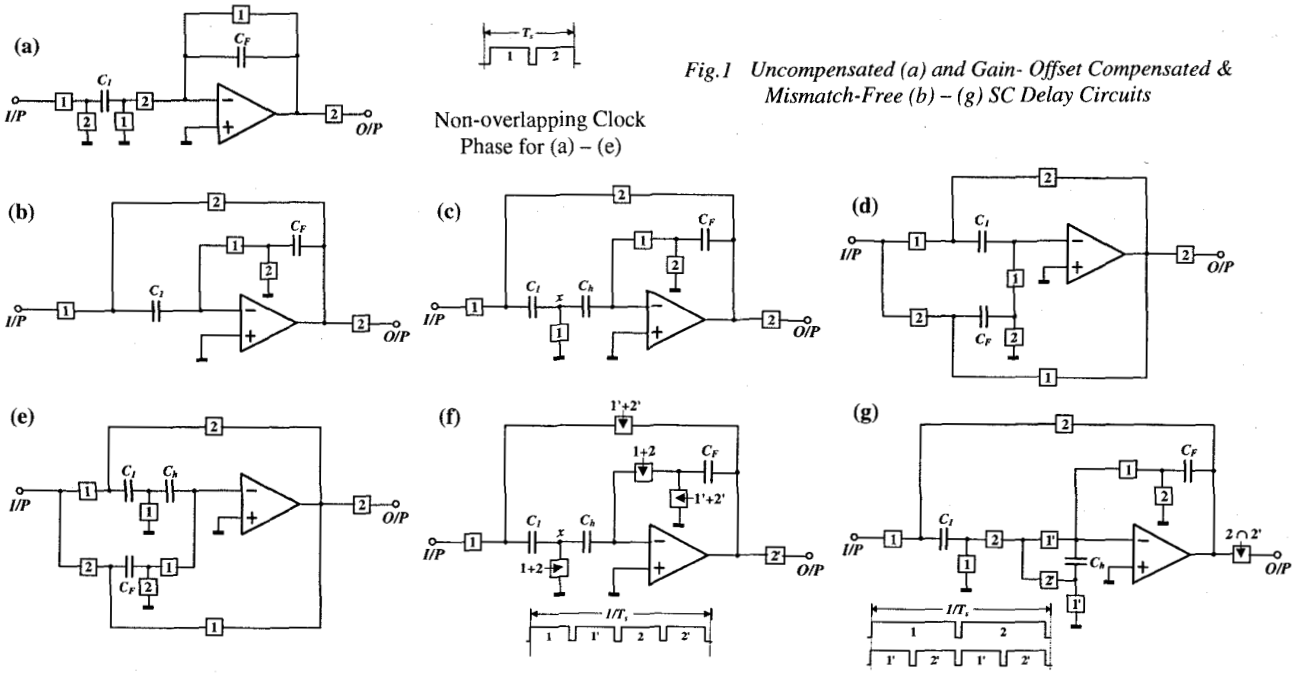


*Fig.1 Uncompensated (a) and Gain- Offset Compensated & Mismatch-Free (b) – (g) SC Delay Circuits*

## 3. CIRCUIT PERFORMANCE WITH THEORETICAL AND SIMULATED RESULTS

To facilitate the comparison of these delay circuits' performance in terms of finite gain compensation, the relative magnitude and phase errors of the overall frequency response will be evaluated. The non-ideal frequency response due to the finite gain can be approximated by [15]

$$H(j\omega) \approx \frac{H_D(j\omega)}{1-m(j\omega)-j\theta(j\omega)}, \text{ when } m(j\omega),\ \theta(j\omega) << 1$$

where the $H_D(j\omega)$, $m(j\omega)$ and $\theta(j\omega)$ are ideal response, gain and phase error of SC delay circuit, respectively. We derive the calculated expressions for these errors of all the above circuits summarized in Table I where $A$ is the finite gain. From here, the ratio $k_1 = C_1/C_F$ for the circuits in Fig.1(b) and (d) is not trivial like $k_h = C_h/C_F$ for those in Fig.1(c), (e) and (f) using offset-storage capacitor, as $k_h$ which normally sets to unity for saving silicon area is correlated to the term $\mu^2$, while $k_1$ is related to the change of $\mu$ that will fairly affect the gain and phase errors. It can be attributed to the extra charge coupling between input sampling and feedback capacitors in circuits Fig.1(b) and (d) during compensated phase mentioned before. Hence, it can be deduced that the performance of circuits Fig.1(b) and (d) will approach closely that of Fig.1(c) and (e) respectively, when $k_1$ becomes smaller. In the similar case of circuit in Fig.1(g), the capacitance ratio $k'_h = C_h/C_1$ should be as small as possible as there is a charge redistribution during the compensated phase, thus rendering a variation of inverting voltage and also the voltage on the sampling capacitor.

For corroborating the effectiveness of these derived expressions and results, the SWITCAP simulation outcomes with respect to both gain and phase errors have been computed in Fig.2(a) and (b) respectively, where finite gain $A$=100 and all related capacitance ratios are unity. The simulated results show excellent agreement with the theoretical, and all circuits exhibit a good compensation in finite gain errors by having the minimum value around 0.0009dB at DC. The anticipatory compensated circuits Fig.1(e) and (f) achieve the highest gain compensation for their smallest, frequency-independent gain and phase errors. When $k_1$ and $k'_h$ are 1, circuits in Fig.1(d) and (g) operate at the similar level of the one in Fig.1(c) in performance, as shown in Fig.2; only when these ratios become smaller, e.g. 0.1, their performance can be comparative to Fig.1(e) (or (f) ) respectively as expected. Similarly, circuit behavior of Fig.1(b) can only be close to that of Fig.1(c) when $k_1$=0.1.

Moreover, the compensation of amplifier DC offset can be manifested in the suppression factor $\gamma$ [12] of offset voltage $v_{os}$ as listed in Table I. All these circuits have similar level of offset suppression $\gamma < 1/A$.Note that all circuits are no longer stray-insensitive due to the finite gain, hence slightly degrading the compensation performance. Moreover, employing offset-storage capacitor in GOC circuits will slightly increase the parasitic effect due to an additional parasitic at the node $x$ connecting capacitor $C_1$ and $C_h$. Indeed, this can be overcome by fairly increasing the input sampling capacitance $C_1$. The simulated gain and phase errors of all the above circuits are further illustrated in Fig.3(a) and (b) when the parasitic capacitance with 10% of the smallest capacitance in the circuits is considered. They clearly show the trivial increase in the magnitude and phase errors of all the above circuits, especially the circuit in Fig.1(c) and (f) due to the above mentioned reason. Besides, in circuit Fig.1(f), the extra error due to the charge division between $C_1$ and the parasitic on its left node during phase 2 can be reduced by inserting a switch between $C_1$ and node $x$. For comparison, Fig.3 also exhibits two additional curves for the circuit Fig.1(c) and (f) with parasitic capacitance 1% of $C_1$.

*Table I : Gain and Phase Errors and Offset Voltage Suppression Factor of Compensated and Uncompensated SC Delay Circuits*

| | Gain Error $m(j\omega)$ | Phase Error $\theta(j\omega)$ | Offset Voltage Error $\gamma$ |
|---|---|---|---|
| **Fig.1(a)** | $-(1+k_1)\mu$ | $0$ | $\frac{(1+k_1)}{1+\mu(1+k_1)}$ |
| **Fig.1(b)** | $-(1+k_1)\mu+\frac{(1+k_1)\mu+k_1\mu^2}{1+\mu}\cos(\omega T_s)$ | $-\frac{(1+k_1)\mu+k_1\mu^2}{1+\mu}\sin(\omega T_s)$ | $\frac{\mu}{(1+\mu)(1+(1+k_1)\mu)}$ |
| **Fig.1(c)** | $-\mu+\frac{\mu}{1+(1+k_h)\mu}\cos(\omega T_s)+\frac{k_h\mu^2}{(1+(1+k_h)\mu)^2}\cos(2\omega T_s)$ | $-\frac{\mu}{1+(1+k_h)\mu}\sin(\omega T_s)+\frac{k_h\mu^2}{(1+(1+k_h)\mu)^2}\sin(2\omega T_s)$ | $\frac{\mu}{(1+\mu)(1+(1+k_h)\mu)}+\frac{k_h\mu^2}{(1+\mu)(1+(1+k_h)\mu)^2}$ |
| **Fig.1(d)** | $-\frac{\mu^2+k_1\mu(1+\mu)(1-\cos(\omega T_s))}{1+2\mu}$ | $-\frac{k_1\mu(1+\mu)}{1+2\mu}\sin(\omega T_s)$ | $\frac{\mu}{(1+\mu)(1+(1+k_1)\mu)}$ |
| **Fig.1(e)** | $-\frac{(1+k_h)\mu^2}{1+(2+k_h)\mu}+\frac{k_h\mu^2(1+\mu)(1+(1+k_h)\mu)(1+(2+k_h)\mu)\cos(\omega T_s)}{(1+(1+k_h)\mu)(1+(2+k_h)\mu)+2k_h\mu^2\cos(\omega T_s)}$ | $\frac{k_h\mu^2(1+\mu)(1+(1+k_h)\mu)(1+(2+k_h)\mu)\sin(\omega T_s)}{(1+(1+k_h)\mu)(1+(2+k_h)\mu)+2k_h\mu^2\cos(\omega T_s)}$ | $\frac{\mu}{(1+\mu)(1+(1+k_h)\mu)}+\frac{k_h\mu^2}{(1+(1+k_h)\mu)^2}$ |
| **Fig.1(f)** | $\frac{(2+k_h)\mu^2+(1+k_h)\mu^3}{1+(3+k_h)\mu+(1+k_h)\mu^2}+\frac{((1+k_h)\mu^2+k_h\mu^3)\cos(\omega T_s)}{(1+\mu)(1+(1+k_h)\mu)(1+(3+k_h)\mu+(1+k_h)\mu^2)}$ | $\frac{((1+k_h)\mu^2+k_h\mu^3)\sin(\omega T_s)}{(1+\mu)(1+(1+k_h)\mu)(1+(3+k_h)\mu+(1+k_h)\mu^2)}$ | $\frac{\mu}{(1+\mu)(1+(1+k_h)\mu)}+\frac{\mu^2}{(1+\mu)^2(1+(1+k_h)\mu)^2}+\frac{k_h\mu^2}{(1+\mu)(1+(1+k_h)\mu)^2}$ |
| **Fig.1(g)** | $-\frac{(k'_h+(1+k'_h)\mu)\mu}{1+2\mu}+\frac{k'_h\mu}{1+(1+k_h)\mu}\cos(\omega T_s)$ | $-\frac{k'_h\mu}{1+(1+k_h)\mu}\sin(\omega T_s)$ | $\frac{k'_h(1+2\mu)\mu+((1+2\mu)-(1+(1+k'_h)\mu))(1+(1+k_h)\mu)}{(1+\mu)(1+(1+k'_h)\mu)(1+(1+k_h)\mu)}$ |

*where* $\mu=\frac{1}{A}$ , $k_1=\frac{C_1}{C_F}$ , $k_h=\frac{C_h}{C_F}$ , $k'_h=\frac{C_h}{C_1}$

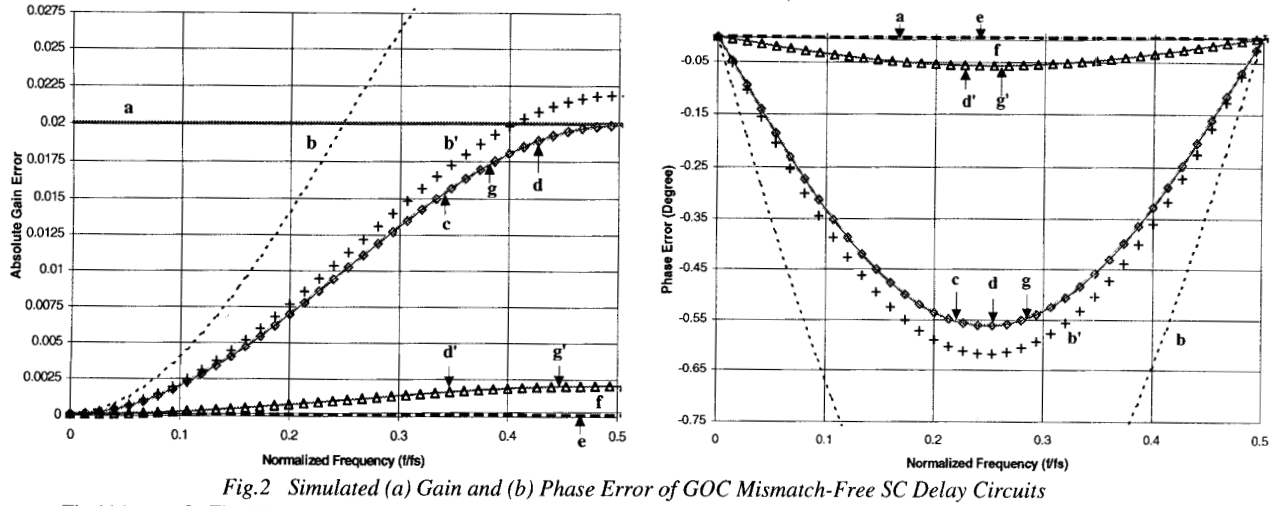


*Fig.2 Simulated (a) Gain and (b) Phase Error of GOC Mismatch-Free SC Delay Circuits*

**a**: Fig.1(a) **b**: Fig.1(b) **c**: Fig.1(c) **d**: Fig.1(d) **e**: Fig.1(e) **f**: Fig.1(f) **g**: Fig.1(g) (all with $k_1=k_h=k'_h=1$)
**b'** : For Fig.1(b) with $k_1 = 0.1$ **d'** : For Fig.1(d) with $k_1 = 0.1$ **g'** : For Fig.1(g) with $k'_h = 0.1$

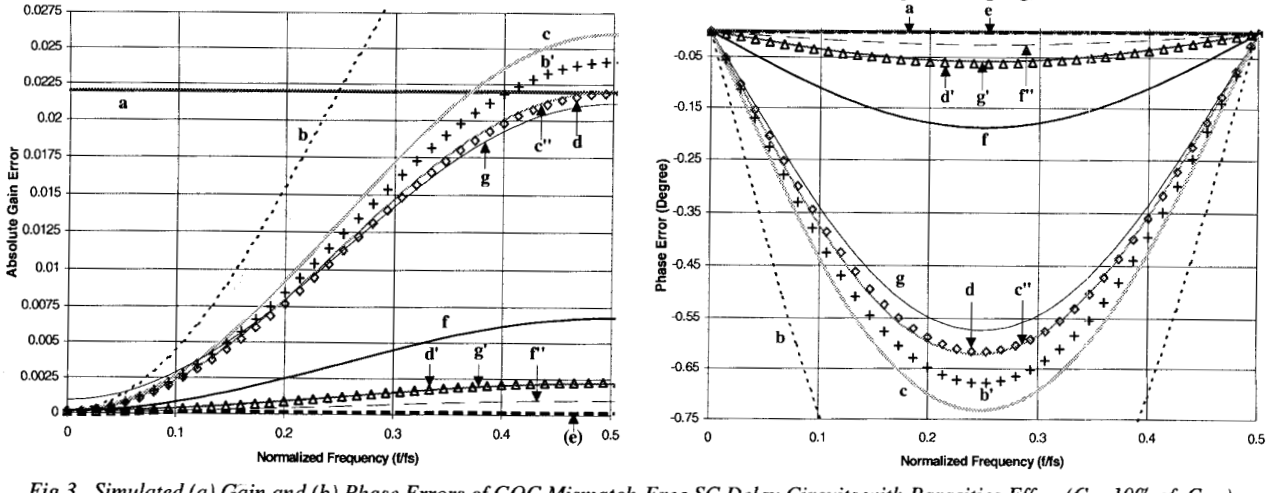


*Fig.3 Simulated (a) Gain and (b) Phase Errors of GOC Mismatch-Free SC Delay Circuits with Parasitics Effec. ($C_p$=10% of $C_{unit}$)*
**a:** Fig.1(a) **b:** Fig.1(b) **c:** Fig.1(c) **d:** Fig.1(d) **e:** Fig.1(e) **f:** Fig.1(f) **g:** Fig.1(g) (all with $k_1=k_h=k'_h=1$)
**b':** Fig.1(b) - $k_1 = 0.1$ **d':** Fig.1(d) - $k_1 = 0.1$ **g':** Fig.1(g) - $k'_h = 0.1$ **c'':** Fig.1(c) - $C_1/C_p$ =100 **f'':** Fig.1(f) - $C_1/C_p$ =100

## 4. LONGER DELAY IMPLEMENTATION

One potential drawback of standard GOC serial delay line is that it normally calls for at least the double number of stages than that of using uncompensated block owing to the ineffective output during compensated phase. Implemented here is a delicate realization of delay blocks for unit or even longer delay with only one amplifier, by employing multiple sampling technique. This is possible when using the offset-storage capacitor scheme. For simplicity, an anticipatory-GOC SC unity delay circuit is derived in Fig.4(a) based on Fig.1(e) with one extra sampling branch and three phases. The penalty of realizing more than unity delay in this type of realization is the doubling of the sampling branches where half of them are used for anticipatory functions. It can be eliminated when modifying the original circuit of Fig.1(c) [16] or Fig.1(g) with the narrow and wideband compensation respectively. Here, only the circuit using Fig.1(g) for realizing double unit delay is presented in Fig.4(b). It can be further applied to achieve delay of $z^{-n}$ with the employment of $n$ input multiplexed SC branches with $n$+2 phases. Most importantly, they require only one amplifier and their compensation performance is exactly the same as those of their original circuits.

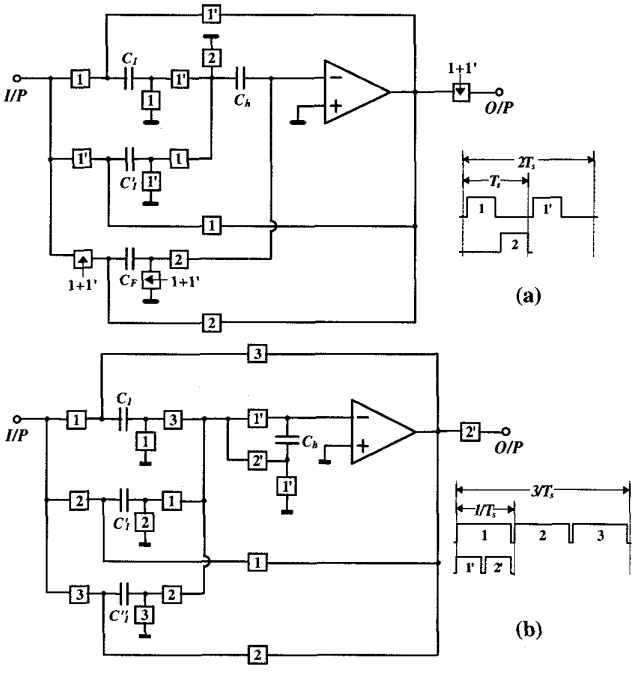


*Fig.4 GOC and Mismatch-Free SC Circuits with Longer Delay*
**(a)** Unit Delay Based on Fig.1(e) **(b)** Double Delay Based on Fig.1(g)

## 5. CONCLUSION

A set of novel mismatch-free SC delay circuits with different finite gain and offset compensation approaches has been proposed and compared. The circuits with anticipatory gain compensation (Predictive CDS), which require more analog components and in some cases multiple clock phases in practice achieve frequency-independent compensation with extremely small gain and phase errors. The offset-storage capacitor compensation approach is relatively superior in precision and also generalization due to the allowance of multiple SC branches; it, however, presents a slightly bigger parasitic effect. The performance of some of the proposed circuits can be considerably improved by adjusting the related capacitor value. Moreover, the parasitic effect of these circuits under finite gain has also been studied. All circuit performance behavior has been verified by both theoretical and computer simulated analyses that match perfectly in outcomes. A practical extension of realization of GOC circuits with unit and longer delay has also been finally investigated by manipulating the different proposed GOC circuit approaches.

### References


[1] P.Gillingham, "Stray-Free Switched-Capacitor Unit-Delay Circuit," *Electronics Letters*,Vol.20,No.7,pp.308-310, 3/1984.

[2] K.Nagaraj, "Switched-Capacitor Delay Circuit That is Insensitive to Capacitor Mismatch and Stray Capacitance," *Electronics Letters*, Vol.20, No.16, pp.663-664, 1984.

[3] A.E.Said, "Stray-Free Switched-Capacitor Building Block That Realizes Delay, Constant Multiplier, or Summer Circuit," *Electronics Letters*, Vol.21, No.4, pp.167-168, 14th Feb.1985.

[4] A.Dabrowski, U.Menzi, G.S.Moschytz, "Offset-Compensated Switched-Capacitor delay Circuit That is Insensitive to Stray Capacitance and to Capacitor Mismatch," *Electronics Letters*, Vol.25, No.10, pp.623-625, 11th May 1989.

[5] Hiroshi Iwakura, "Realization of Tapped Delay Lines Using Switched-Capacitor LDI Ladders and Application to FIR Filter Design," *IEEE Trans. on CAS-II*, Vol.40, pp.794-797, Dec.93.

[6] U Seng Pan, R.P.Martins, J.E.Franca, "Intermittent Polyphase SC Structures for FIR Rational Interpolation", in *Proc. IEEE ISCAS'97*, pp.121-124, Hong Kong, Jun.1997.

[7] Seng-Pan U, R.P.Martins, J.E.Franca, "Impulse Sampled FIR Interpolation with SC Active-Delayed Block Polyphase Structures," *Electronics Letters*,Vol.34, No.5, pp.443-444, Mar.98.

[8] K.Haug, F.Maloberti, G.C.Temes, "Switched-Capacitor Integrators with Low Finite-Gain Sensitivity," *Electronics Letters*, Vol.21, No.24, pp.1156-1157, 21st Nov.1985.

[9] L.E.Larson, G.C.Temes, "Switched-Capacitor Gain Stage with Reduced Sensitivity to Finite Amplifier Gain and Offset Voltage," *Electronics Letters*, Vol.22, pp.1281-82, Nov.1985.

[10] K.Nagaraj, K.Singhal, T.R.Viswanathan, J.Vlach, "Reduction of Finite-Gain Effect in Switched-Capacitor Filters," *Electronics Letters*, Vol.21, No.15, pp.644-645, 18th Jul.1985.

[11] K.Nagaraj, T.R.Viswanathan, K.Singhal, J.Vlach, "Switched-Capacitor Circuits with Reduced Sensitivity to Amplifier Gain," *IEEE Trans. on CAS*, Vol.CAS-34,pp.571-574, 5/1987.

[12] Wing-Hung Ki, G.C.Temes, "Offset-Compensated Switched-Capacitor Integrator," in *Proc. IEEE ISCAS'90*, pp.2829-31.

[13] H.Shafeeu, A.K.Betts, J.T.Taylor, "Novel Amplifier Gain Insensitive Switched Capacitor Integrator with Same Sample Correction Properties," *Electronics Letters*, Vol.27, No.24, pp.2277-2279, Nov.1991.

[14] Y.Huang, P.Ferguson, G.C.Temes, "Reduced Nonlinear Distortion in Circuits with Correlated Double Sampling," *IEEE Trans. on CAS-II*, Vol.44, No.7, pp.593-597, Jul.1997.

[15] K.Martin, A.S.Sedra, "Effects of the Op-Amp Finite Gain and Bandwidth of the Performance of Switched-Capacitor Filters," *IEEE Trans. on CAS*, Vol.CAS-28, pp.822-829, Aug.1981.

[16] Seng-Pan U, R.P.Martins, J.E.Franca, "Offset- & Gain-Compensated and Mismatch-Free SC Delay Circuit with Flexible Implementation," *Electronics Letters*, in press.