# HIGH-FREQUENCY LOW-POWER MULTIRATE SC REALIZATIONS FOR NTSC/PAL DIGITAL VIDEO FILTERING

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## ABSTRACT

This paper proposes a cost-efficient multirate Switched-Capacitor structure and its realization for a high-frequency low-power sampled-data anti-imaging filter with 108 MHz output sampling rate for CCIR-601 NTSC/PAL digital video. The filter employs a 2-stage (8-tap + 6-tap) improved multirate FIR polyphase structure with double-sampling techniques to achieve the desired linear-phase filtering with 5 MHz-corner passband (<±0.25 dB ripple) and 22 MHz-corner stopband (>40 dB attenuation) as well as an embedded sampling rate increase from 27 MHz to 108 MHz. The circuit, designed with 0.35 μm CMOS technology, is expected to consume only about 28 mW for the analog part at 3.0 V supply.

## 1. INTRODUCTION

The increased demands of digital video in contemporary consumer and professional applications, like DVD players, TV-output in DVD-equipped PCs, PC multimedia video editing systems, digital set-top boxes, digital still cameras, video phones as well as studio and broadcast video systems and so on, require a high integration of the large digital system with traditionally external analog interfaces on a single chip to achieve a high-performance and economic implementation. However, many currently available video encoders in the market still require an external passive inductive-capacitive (LC) filter for post anti-imaging filtering to the standard analog composite (NTSC or PAL) or S-video outputs for rejecting the images from the inherent sampling process in digitizing analog video [1-4]. The implementation of high-order monolithic continuous-time (C-T) filters together with phase-equalization for wideband video applications is still not straightforward and cost-efficient due to the limitation of the inherently inaccurate time-constant in current IC technology [5-6].

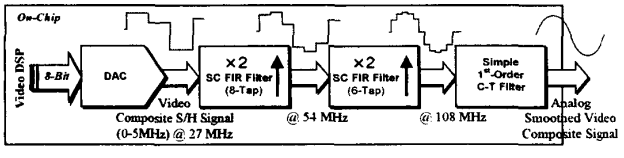


Fig.1 Low-cost analog interface for digital video by 2-Stage SC FIR anti-imaging filter

This paper presents a realization of a power-efficient Switched-Capacitor (SC) anti-imaging filter operating at the input sampling rate of 27 MHz according to the NTSC/PAL digital video encoding standard [1-4], but with a 4-fold higher sampling rate at the output, i.e. 108 MHz, to allow a very relaxed 1st-order continuous-time post filter, e.g. -3dB-frequency can be varied within ±20% around the nominal 18 MHz, thus leading to a low-cost full single-chip alternative, as shown in Fig.1.

Due to the inherent linear-phase and less sensitivity properties in the passband, sampled-data or SC FIR filtering is a very attractive technique for those video applications with standard 8-bit accuracy [7-9]. However, it is still problematic in real circuit implementation for high-frequency and high-order filtering since it results in large capacitance spread, increased sensitivity to the capacitance ratio errors, the imperfections of Operational Trans-conductance Amplifiers (OTA's), e.g. finite gain & bandwidth and offset errors, and also to non-ideal analog switches, e.g. non-zero $R_{on}$, charge-injection and clock-feedthrough errors. All those effects will be analyzed within the design of this SC filter that embeds an increase of the sampling rate, or designated as SC interpolator. It achieves a typical digital video CCIR-601 standard for NTSC/PAL signals with a linear-phase, 5 MHz equi-ripple passband (<±0.25 dB, no need for S/H compensation) and a 40 dB rejection stopband. The 0.35 μm CMOS double-poly triple-metal technology is employed for the design taking into account all of those imperfections aforementioned.

## 2. SC DESIGN AND IMPLEMENTATION

### 2.1 Circuit Structure with Spread Reduction

For traditional design, this filter not only needs to be inefficiently operated at higher output 108 MHz sampling rate, which results high power and area dissipation with significantly degraded performance, but also suffers from the extra 0.6 dB passband rolloff due to the sample-and-hold (S/H) effect at lower input sampling rate, as well as the impractical more-than-450 capacitance spread. The specialized, multirate polyphase non-recursive structures are inherent suitable for high-frequency operation due to the very relaxed speed need of active analog devices, i.e. OTA's, the elimination to input S/H effect, as well as the reduced spread (450/L=112.5, L is the rate increase ratio) [10]. However, this 112.5 spread is still too large for implementation not only because of the inefficient area and increased sensitivity but also a very heavy capacitive loading to the OTA's that will limit their high-frequency operation. Though some techniques, like T-cell or split-integrating capacitor, can be used in the case of large capacitor ratio, they either suffer from the parasitics or the reduced settling time of OTA's. Here, the spread of only 16 is achieved finally with the employment of a two-stage (8-tap + 6-tap) cascade multirate FIR realization.



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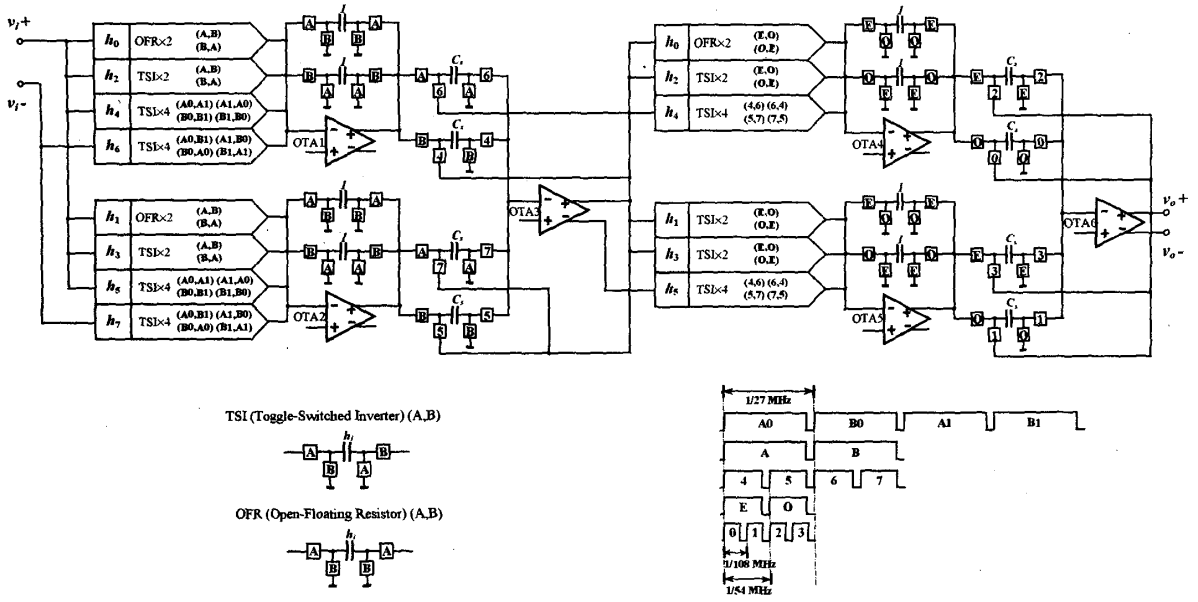


Fig.2 Simplified schematics and clock phases of 2-Stage SC FIR video anti-imaging filter

For simplicity, the original fully-differential circuit has been simplified and is shown in Fig.2. The input S/H stage is not mandatory since the input signals of the circuit from the DAC usually are already sampled-and-held at 27 MHz, and it will be only needed for buffering, if the DAC has not enough driving capability to the required capacitive loading. Moreover, due to the low-speed nature of the polyphase structure, the efficient parallel realization of SC coefficient branches is employed without paying too much in terms of area and clock phases. Here, only less than half of the coefficients are implemented by double SC branches for achieving their corresponding delay. Thus, the net resulting increased number of phases are only A0, A1, B0 and B1 which can be easily obtained from phase A and B by simple digital logic. The extra power, mainly occupied from their buffers for driving switches operating at the lowest input frequency, is considerably minor as they lessen the power of the buffers for phase A and B. When compared to active OTA-based tapped delay line approach, this offers a better performance in terms of power, accuracy, finite gain and bandwidth, as well as offset propagation sensitivities with the cope of the employment of even number of FIR filter taps, which will be discussed next.

## 2.2 OTA Structure and Speed Assignments

Multirate non-recursive polyphase structures decompose the transfer function of each stage into L=2 sub-polyphase filters each being responsible for generating one of L output samples at the lower input sampling rate. To take advantage of this low-speed operation nature, L=2 individual output accumulators are used for each polyphase filter. For further improvement, double-sampling techniques are also employed in all polyphase filters, thus leading to a wider full input sampling period settling time for the OTA's, e.g. maximum of 37 ns and 18.5 ns for accumulators in 1st- (OTA1 & 2) and 2nd-stage (OTA4 & 5), respectively, which are indeed 4 and 2 times longer than those of OTA's if traditional realization with double sampling is used. This also contributes to the reduction of the noise, charge-injection and clock-feedthrough errors and especially a more freedom headroom for the design of high-frequency OTA's. Although only one output multiplexer (OTA6) operates with 9.25 ns settling time (full output period) to switch the interpolated output from the 2 polyphase filters, the feasibility is derived from the fact that specifications of the multiplexer OTA is much less stringent than that in accumulators, if operating at the same speed. Because first, due to the elimination of the charge transferring, the OTA always operates with a large feedback factor (> 0.5 when the sampling capacitor is greater than input parasitics capacitance of OTA), thus reducing the bandwidth requirement. Normally, the relatively smaller total equivalent capacitive loading compared with those formed by a set of coefficient capacitors (for OTA's in S/H) with also a large summing feedback capacitor (for OTA's in accumulators), together with usually smaller output voltage step during two consecutive phases (due to the sampling rate increase nature), usually relax the Slew-Rate (SR) and transconductance requirements which are directly proportional to the power consumption of OTA's. If it is necessary to drive a resistive or large capacitive load, then buffers with low output-impedance are normally required for better performance in the OTA-based analog circuit. The power assignment of the OTA's in the circuit is presented in Table I, which shows that the power requirement

of the last multiplexer OTA6 is quite similar to the OTA's of accumulators (OTA4 & 5) which all have twice settling time of OTA6. The only one power-consuming element is the OTA3 in the multiplexer of the 1st-stage, due solely to the need to drive large capacitive loading imposed by all 2nd-stage coefficient capacitors. Note that the elimination of charge-transfer in the multiplexer reduces not only the mismatch errors for each path but also the special glitches, which normally will appear in the beginning of the charge-transfer in OTA-based SC circuits, due to the OTA high output-impedance, thus again rendering a reduced OTA SR.

Table I Power and speed assignments of OTA's in circuit

| | Stage 1 | | Stage 2 | |
|---|---|---|---|---|
| **OTA** | **1 & 2** | **3** | **4 & 5** | **6** |
| ***Settling Time**** | 35 ns | 16.5 ns | 16.5 ns | 7.25 ns |
| ***Max.* $V_{o\text{-}step}$** | 1.2 V | 0.7 V | 0.7 V | 0.4 V |
| ***SR*** | 200 V/μs | 300 V/μs | 250 V/μs | 320 V/μs |
| ***FB Factor*** | 0.33 | 0.53 | 0.36 | 0.58 |
| ***Equivalent*** $C_L$ | 4.7 pF | 7.5 pF | 4.4 pF | 3.6 pF |
| $g_m$ | 2.8 mS | 6 mS | 5.2 mS | 6.1 mS |
| $I_{SS}$ | 1 mA | 2.2 mA | 1.1 mA | 1.2 mA |
| ***No. of Use*** | | ×1 | | ×5 |

* Note : 2 ns is allocated for Non-overlapping phase gap and delay time for clock-delayed sampling technique

Since the video signal swing is typically 1 $V_{p\text{-}p}$, simple single-stage telescopic OTA structure with Miller-effect cancellation transistors and wide-swing, internal-biasing for the cascode transistors is adopted here for its superior high-speed and low-power capability. The common-mode voltage is stabilized at 1.1 V by a dynamic SC common-mode feedback circuit. For simplicity, only two different OTA's (one with 6.6 mW of power and another with 3.6 mW) are designed for the circuit and the worst-case Cadence Spectre simulated results meet well the minimum specifications listed in Table I.

### 2.3 NMOS-Only Switch Assignment

For high-frequency SC circuits, non-zero switch resistance will not only affect the sampling charge errors but, more importantly, the settling time of OTA's due to its resulting degradation in the closed-loop pole of the overall structure. The different-level effect will be introduced by the switches in the sampling branch and the feedback summing branch, where a too small switch causes more sampling errors and reduces the phase margin for the OTA, while a too large switch introduces large charge-injection and clock-feedthrough errors, so an optimized size of switches is important and they can even be used for improving the settling time of OTA. Here, all switches are sized from maximum 25/0.3 to 1/0.3 to accommodate the different loading conditions with the consideration of the above effects. The clock-delayed with fully-differential technique is used to reduce the signal-dependent charge-injection and clock-feedthrough errors. To not only relax the circuit complexity but simplify the required clock phases, only NMOS switches are used in this circuit owing to the low common-mode voltage level.

## 3. SIMULATION RESULTS WITH NON-IDEAL EFFECTS

### 3.1 Capacitance-Ratio Mismatches Effects

The computer-based Monte-Carlo frequency response simulation with respect to all capacitance ratios which are independent zero-mean Gaussian random variables with the deviation within 1.5 % (or $\sigma_e$ = 0.5 %) has been performed according to this two-stage cascade circuit implementation. Due to the low sensitivity nature in the passband from FIR structure, the resulting passband ripple presented in Fig.3 shows that it is smaller than 0.3 dB and the upper and lower bound, to its shifted deviations, are all within desired ±0.25 dB without any compensation to the output S/H shaping effect. Such small passband ripple is also attributed to the inherent elimination of the input S/H effect aforementioned in our structures. It is obvious that the unwanted image bands located at 27 MHz, 54 MHz and 81 MHz have been attenuated by the 1st- and 2nd-stage subsequently with greater than 43 dB. Note that the simple direct capacitance ratio for each coefficient in the SC circuit realizations and especially the cascaded implementation help to lessen the sensitivity to the process variation. Besides, instead of using the traditional normalization of all capacitor coefficients with respect to the minimum one, we normalize the biggest summing capacitor to its nearest integer and adjust the coefficients for the purpose of making the most sensitive tap weight, like the mid-coefficient, to have an integer ratio to the summing capacitor, thus achieving a better matching in layout due to the elimination of its non-unit capacitor part. Note that the extra image noise tones due to the mismatches among the parallel coefficients, similarly happened in standard double-sampling SC circuits, can be normally neglected by using proper layout technique, like common-centroid with dummy surrounding, as the simulation shows that 5 % mismatching imposes the images with lower than -50 dB level.

### 3.2 OTA Finite Gain & Bandwidth Effects

The errors due to the finite gain and bandwidth of OTA's indeed lead to the impulse response coefficient deviation, and in turn affect the frequency response of the overall filter. Elimination of the active error-accumulated delay-line is an effective way to reduce such effect. However, the polyphase filters operate in parallel, so the gain and bandwidth mismatches in two paths will worsen such deviation. For the case with 2-fold interpolation ratio, we adopt the even-number FIR filter taps so that each path has the same weighted-coefficient branches and equivalent capacitive loading. Thus, their corresponding symmetrical layouts can be made in a more faster and easier way but with better matching. The computer simulations shown in Fig.4 (obtained by using one-pole OTA model including input and output parasitics with nominal $g_m$ in Table I, gain of 1000 and also the top (10%) & bottom (30%) parasitics in all capacitors and the corresponding non-zero switch on-resistance) indicate that the 25 % reduction of $g_m$ in both of the two accumulator OTA's (equivalent to 25 % deviation to both gain and speed) is better than 25 % deviation in only one path. However, both responses still meet the desired specifications well. Moreover, the gain and offset of multiplexer OTA's (OTA3 & 6) generate mainly the gain response shift and output signal DC offset.

### 3.3 Offset-Noise Tone Effects

The mismatch of the offsets caused by the OTA's and switch charge-injection and clock-feedthrough in two low-speed poly-phase filters introduces a notable degradation to the Signal-to-Noise Ratio (SNR) due to their input-signal-independent fixed pattern noise tones. This is one of the important error sources especially for sampling rate increase system, as those tones lay on the lower sampling rate and its multiples that indeed overlap onto the sampling images band of input signals, i.e. 27, 54 and 81 MHz, but can't be suppressed by the interpolation filter. Here, such noise tones depend on the mismatch of the offset of OTA's in two polyphase paths rather than the net value due to the even-number filter tap and delay-line-free structure. Ideally, they can be eliminated if two paths are perfectly matched and the simulation shows that a 10 mV offset mismatch in two path OTA's, which can be controlled in current technology with proper layout, results in noise tones around -45 dB.

## 4. CONCLUSIONS

This paper has presented an efficient structure, design and implementation of a low-power 27 MHz to 108 MHz 2-stage SC FIR interpolation filter for post image rejection of CCIR-601 NTSC/PAL digital video. Special issues to this high-frequency analog filter in terms of the required OTA power and speed, sensitivity to finite gain and bandwidth, the offset pattern noise effects and the capacitance ratio mismatches as well as the non-ideal analog switches have been addressed on the basis of the computer simulation analysis. The circuit, designed with 0.35 μm CMOS, is expected to consume an active area and overall power, including the digital part, of less than 2.5 $mm^2$ and 60 mW, respectively, at 3V supply (28 mW for analog part with input S/H stage), which is attractive when compared to more than 250 mW in typical analog video filter products [11].

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ACKNOWLEDGEMENT – This work was supported in part by the Research Committee of the University of Macau and the Fundação Oriente.


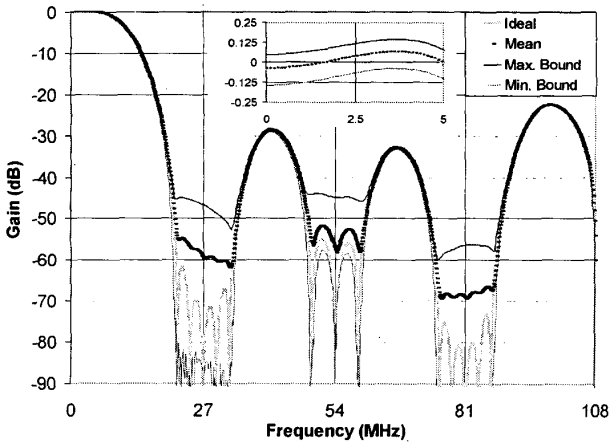


Fig. 3 Capacitance ratio mismatches effect for 2-stage SC anti-imaging filter – 1000-time Monte-Carlo amplitude response simulations ($\sigma_e$ = 0.5 %)

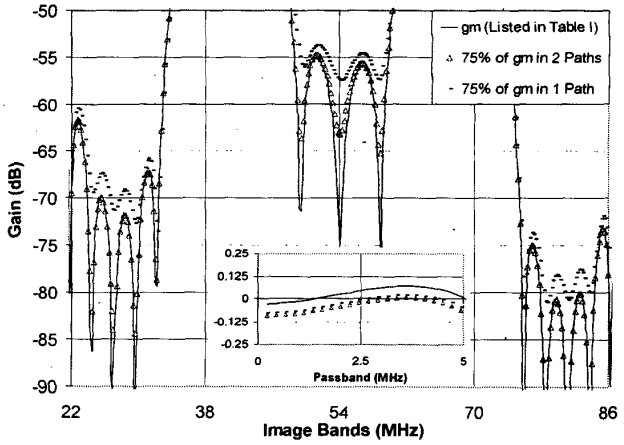


Fig. 4 OTA finite gain and bandwidth effects for 2-stage SC anti-imaging filter – Amplitude response simulations with one-pole OTA model, parasitcs capacitance of OTA, SC branches and non-zero switch resistance