Comparator with Built-in Reference Voltage Generation and Split-ROM Encoder for a High-Speed Flash ADC

Yong Chen [1], Pui-In Mak [2], Jiale Yang [1], Ruifeng Yue [1] and Yan Wang [1]

1 – Institute of Microelectronics, Tsinghua University, Beijing 100084, China
2 – The State-Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macao, China

***Abstract*—Two circuit techniques for performance enhancement of high-speed flash ADCs are proposed. A calibration-intensive dynamic comparator features an improved built-in reference voltage generation scheme to alleviate the issue of kickback noise, and a proper reset function to clean the memory effect due to the dielectric relaxation in the capacitors, yielding better static and dynamic linearity performances. The second is a split-ROM encoder, which halves the signaling path to lower the parasitics, while boosting the back-end processing speed with small power. The feasibility of them is demonstrated via a 5-bit flash ADC designed in 65nm CMOS. With 3.69mW of power, the ADC operated at 2GS/s exhibits an ENOB of >4.5 bits up to an ERBW of 3.6GHz. The DNL and INL are within +0.091/–0.071 and +0.066/–0.062 LSB, respectively.**

I. Introduction

With the trend towards lower power and higher data rate in portable wireless devices, several standards based on the 60-GHz carrier frequency have been proposed, being one of the most promising short-range wireless technologies in the years to come [1, 2]. For their baseband interfaces, a very-high-speed medium-resolution analog-to-digital converter (ADC) is required. The flash architecture is the most common high-speed ADC, owing to its instantaneous signal comparison and output. Yet, its drawback is the exponential relationship between the number of comparators and size of the resistor reference ladder with the resolution of the ADC. Most prior arts [3-5] were not able to optimize the power due to the use of pre-amplifiers to suppress the comparator's dc-offset and kickback noise injected to the reference ladder. Alternatively, calibration-intensive dynamic comparators [6-8] with built-in reference voltage generation are preferred, avoiding both pre-amplifiers and reference ladders that are the most power hungry. Still, this kind of dynamic comparator is normally based on asymmetrical widths of input transistor to generate those built-in reference voltages, leading to significant kickback noise affecting the input signal [9].

This paper describes a flash ADC with two new circuit techniques. The first is a dynamic comparator with improved built-in reference voltage generation and proper reset function. The former effectively reduces the kickback noise, while the latter enhances both static and dynamic linearity performances of the ADC via addressing the dielectric relaxation in the capacitors [10-12]. The second technique is on the back-end digital part. A split-ROM encoder is proposed to effectively halve the signaling path and decrease the parasitic capacitance, resulting in higher speed of operation at lower power. The feasibility of the two techniques is demonstrated in a 5-bit 2GS/s flash ADC optimized in a 65nm CMOS.

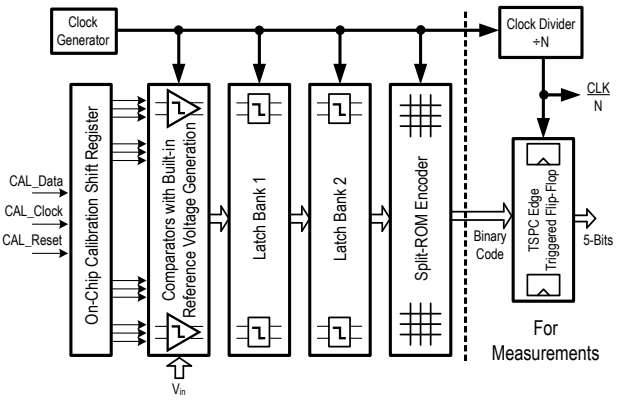

Fig. 1. A 5-bit 2-GS/s flash ADC architecture.

II. Low-Power High-Speed 5-Bit Flash ADC

The block diagram of the flash ADC is depicted in Fig. 1. To optimize the speed-to-power efficiency, there is no front-end track-and-hold circuit and pre-amplifiers. The input signal is directly sensed by the 31 comparators with built-in reference voltage generation. The simplified signal path further incorporates two set-reset (SR) latch banks, a digital encoder based on split ROM, and an edge-triggered flip-flop latch bank. All of them share a common on-chip clock generator. The use of two latch banks in cascade enhances the regenerative gain to minimize the chance of metastability. The digital encoder is based on quasi-gray split ROM in order to correct the bubble errors with simple logic operation. An edge-triggered flip-flop latch bank is located at the end of the ADC for sub-sampling the binary code by 1/N of the clock frequency for measurements.

The on-chip calibration shift register is to adjust the reference voltages of all comparators such that their offsets are minimized. Every comparator features a 16-bit digitally-controlled capacitor. The calibration range is proportional to the size of the total control capacitance, and the calibration step is determined by the minimum MOS capacitance $\Delta C_{step,calibration}$ whose size is 120 x 60 nm. Their relation is given as follows,

$$C_{total,calibration} = 2N \times \Delta C_{step,calibration} \quad (1)$$

where N is from 0 to 16. The on and off states of every capacitor calibration bit are controlled by the digital voltage that locates in the bidirectional shift register. Corresponding to every calibrated comparator, a bidirectional shift register array stores the control code composed of two groups of 16 digital voltages that control the positive and negative calibrated capacitor arrays. A serial calibration input modifies the data in a certain bidirectional shift register for calibrating the corresponding comparator, which is

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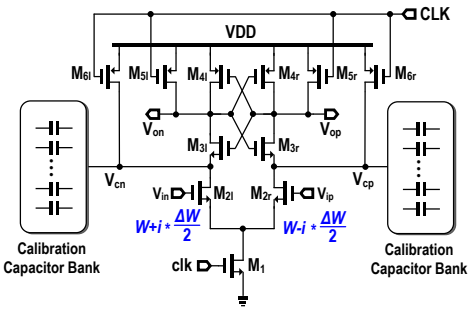


Fig. 2. The conventional dynamic comparator. The built-in reference voltages are generated by width scaling of the input transistor pair.

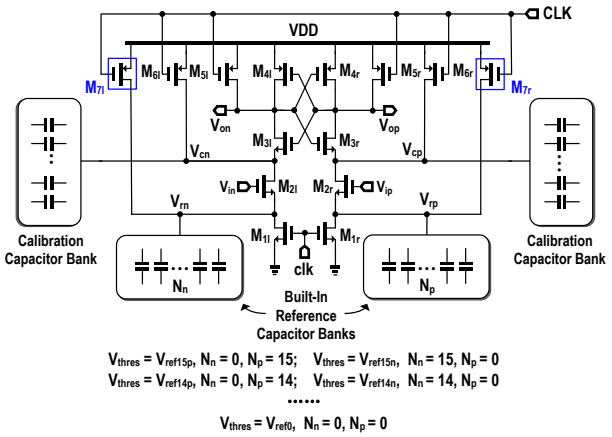


Fig. 3. The proposed dynamic comparator. The built-in reference voltages are generated by another capacitor bank located at the source node of the input transistor pair. The reset switch M_{7l} (M_{7r}) at V_{rn} (V_{rp}) enhances the linearity performances significantly.

chosen by a demultiplexer. The calibration address codes are given off-chip from a computer with a USB-to-SPI interface.

III. Conventional and Proposed Dynamic Comparators

Conventional dynamic comparators regenerate the differential voltage at the input of the latch, which is given by the current difference of the input transistor pair. Moreover, the reference voltage is provided by a resistor ladder that undesirably consumes static power.

A better alternative is the calibration-intensive dynamic comparator shown in Fig. 2, which features built-in reference voltage generation. There are two operating phases (reset and comparison). After a falling clock edge has turned on the switch transistors (M_{5l}, M_{5r}, M_{6l} and M_{6r}), the comparator will enter into the resetting phase, i.e., V_{op} V_{on}, V_{cn} and V_{cp} are reset to VDD. After a rising clock edge turns on the switch transistors M_{1l} (M_{1r}), the comparator will enter into the comparing phase and the input voltage is sampled by the input transistor M_{2l} (M_{2r}). The latch function consists of two cross-coupled inverters (M_{3l} and M_{3r}, M_{4l} and M_{4r}) are discharged through M_{2l} and M_{2r}, where the slew rate depends on the applied input voltage and the width of the input transistor. Then, the latch regeneratively amplifies any differential voltage present on the regeneration node (V_{cn} and V_{cp}) to a rail-to-rail voltage. The digitally controllable capacitance is connected to the drain node of M_{2l} (M_{2r}), i.e., V_{cn} (V_{cp}).

Intentional offset can be added to the dynamic comparator as built-in reference voltages to replace the role of the reference ladder. A conventional comparator with built-in reference voltage is set by changing the width of the input transistor, as illustrated in Fig. 2. The shift of the trip point of the comparator generated by the asymmetrical width of input transistor is given by,

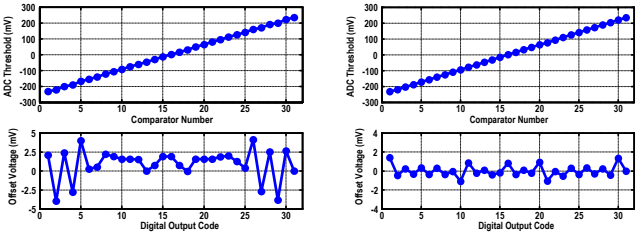


Fig. 4. The comparator's built-in reference voltages (a) without and (b) with the reset switches.

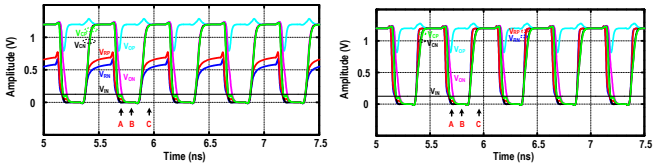


Fig. 5. Simulated internal node voltages of the comparator under a 125-mV DC input: (a) without and (b) with the reset switches.

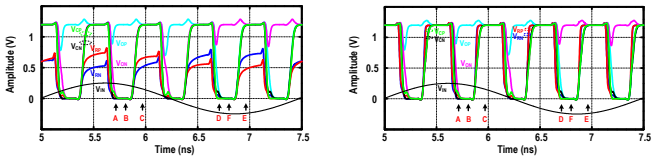


Fig. 6. Simulated internal node voltages of the comparator under a sine input ($500mV_{pp,diff}$ and F_{in} = 401.1MHz): (a) without and (b) with the reset switches.

$$\Delta V_{level,i} = \frac{i \times \Delta W}{W} \frac{I_{M2}}{g_{m,M2}} \approx \frac{i \times \Delta W}{W} \frac{V_{GS,M2} - V_{th}}{2} \qquad (2)$$

where i varies from $-(2^{N-1} - 1)$ to $(2^{N-1} - 1)$ for $2^N - 1$ reference voltage levels. The reference voltage is tuned to the desired value by setting different calibration capacitances connected to V_{cn} (V_{cp}). The comparator works fast and consumes less power. However, the asymmetrical width of input transistors would result in highly imbalanced input capacitance. Differential kickback noise from regeneration node will be injected to the input node V_{in} (V_{ip}) of the comparator, degrading the effective resolution of the ADC.

Unlike the abovementioned comparator that is based on asymmetrical width of input transistors to generate the built-in reference voltages [13], the proposed dynamic comparator (Fig. 3) connects the calibration capacitors at the drain node of M_{2l} (M_{2r}), but the built-in reference capacitors are connected at the source node of M_{2l} (M_{2r}), i.e., V_{rn} (V_{rp}), such that the width of M_{2l} (M_{2r}) involves no scaling. The intentional offset is generated by different capacitance ΔC at V_{rn} (V_{rp}), which can be given by,

$$\Delta V_{level,i} = \frac{i \times \Delta C}{C} \frac{I_{M1}}{g_{m,M1}} \approx \frac{i \times \Delta C}{C} \frac{V_{GS,M1} - V_{th}}{2} \qquad (3)$$

Also, differing from the conventional comparator, there are two more reset switches M_{7l} (M_{7r}) added to clean V_{rn} (V_{rp}) during every clock cycle. For a 5-bit ADC with 31 comparators, it is feasible to optimize each reference level via tailoring the capacitance at the source node of the input transistor pair during the design phase. The built-in reference levels and offset without and with the reset switches are plotted in Fig 4(a) and (b), respectively. For the former, the offset voltage is within –4.0 to 4.1mV, but is reduced to –1.1 to 1.4mV in the latter. This result corresponds to an improved LSB resolution of 16.7 mV excellent for a 5-bit resolution target. For their differences in dynamic performances, time-domain simulations were conducted as described next.

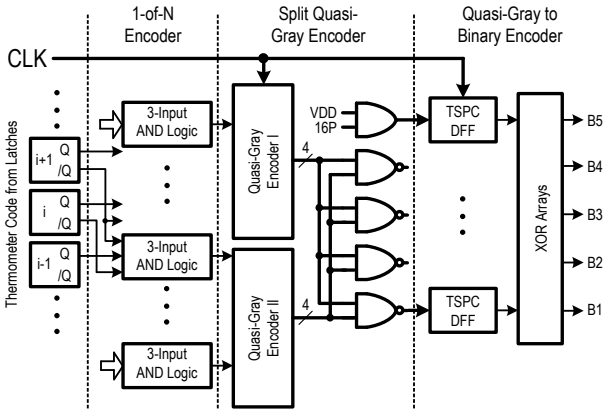


Fig. 7. Proposed Split-ROM encoder.

The dielectric relaxation in the parasitic and load capacitors at V_{rn} (V_{rp}) will cause a memory effect in the comparator. Thus, to improve the dynamic performances, one effective way is to reset the voltage at V_{rn} (V_{rp}) every clock cycle. A few illustrative examples are given next.

When a DC voltage (125mV) is inputted to the comparator without [Fig. 5(a)] and with [Fig. 5(b)] the reset switch, we can observe the voltages at different sampling times. At around A point, M_{1l} (M_{1r}) is turned on, the voltage difference ($V_{cp} > V_{cn}$) between V_{cp} and V_{cn} is set up, and the cross-coupled latch will regeneratively amplify the voltage difference. At around B point, the voltages at V_{op} (V_{on}) is put to VDD (VSS). Beginning around C point, the two comparators will be in the reset phase. If there is no reset switch, the voltages at V_{rp} and V_{rn} are unequal and cannot be well defined. In contrast, after proper reset, the voltage at V_{rp} (V_{rn}) is always VDD. These differences can be labeled at around 5.5, 6, 6.5 and 7ns.

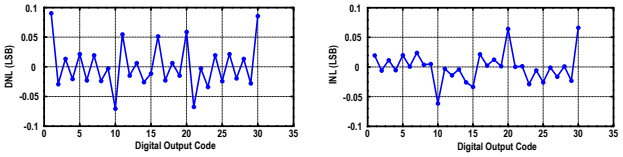
When a sine signal (V_{in} = 500m$V_{pp,diff}$ and F_{in} = 401.1MHz) is used as test source, the voltage at the adjoining sampling time is different. The simulation results without and with the reset switches are shown in Fig. 6(a) and (b), respectively. The results at the A, B and C points are similar to those under a DC input. At around D point, M_{1l} (M_{1r}) is turned on, while the voltage difference ($V_{cp} < V_{cn}$) between V_{cp} and V_{cn} is set up according to the negative sine input signal that is less than zero. The cross-coupled latch will regeneratively amplify this voltage difference. At around F point, the voltages at V_{op} (V_{on}) is put to VSS (VDD). Beginning around E point, the two comparators will be in the reset phase. Again, with the reset switch, the voltage at the node V_{rp} (V_{rn}) can be well defined at VDD.

IV. Proposed Split-ROM Encoder

Figure 7 shows the proposed encoder using a split-ROM scheme. The thermometer code generated from SR latch bank is encoded into binary code with two splitting ROM encoders, where a 1-of-N encoder is followed by two splitting Quasi-Gray ROM encoders and Quasi-Gray to Binary encoder. The 1-of-N encoder consists of three-input AND gates that sense every three consecutive bits of thermometer code and generate a ONE only if the upper two bits are ZEROs and the lower bit is ONE, which can detect sparkles and perform a first-order correction, generating a true 1-of-N code if the thermometer code has only one sparkle. Every splitting ROM encoder is composed of bit line, word line and memory cells, where by a given address code from input bit line Quasi-Gray code can be generated on word line based on pre-stored information in the ROM. Each cycle the word lines are pre-charged by PMOS transistors gated by clock signal, and discharged by NMOS transistors when needed gated by 1-of-N code. Splitting up the ROM encoder into two halves the signaling path and decreases the parasitic capacitance so that the speed is greatly increased. The four two-input NAND gates combines the two groups output from two splitting ROM encoders to generate the lower 4-bit binary codes. The most significant bit is created from the positive signal of the sixteen SR latches and VDD. The conventional encoder can reduce glitch noise, but it needs an excessive amount of conversion time to get a 5-bit binary code output. To reduce the conversion time, a quasi-gray code is implemented with the following conversion,

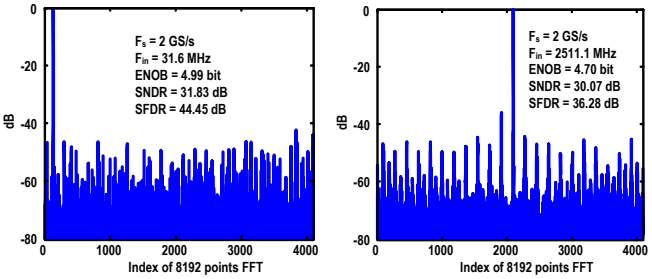
$$c(i)+c(i+1)=b(i)$$
$$c(M)=b(M) \quad (4)$$

where b(i) is the i-th bit of output binary code, c(i) is the i-th bit of the quasi-gray code, and M means the most significant bit (MSB). This conversion is implemented with two-input XOR gate array.



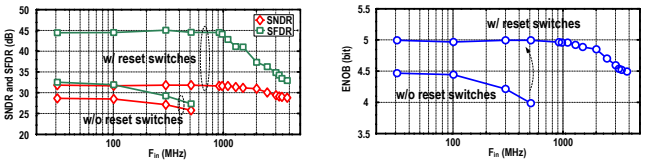
(a) (b)

Fig. 8. Simulated (a) DNL and (b) INL of the designed flash ADC.



(a) (b)

Fig. 9. Simulated output spectrum of the ADC at an input signal frequency of (a) 31.6 MHz and (b) 2511.1 MHz.



(a) (b)

Fig. 10. Simulated (a) SNDR and SFDR and (b) ENOB versus F_{in} with and without the reset switches. The sampling frequency is 2 GHz.

V. Simulation Results

The proposed comparator and encoder are applied in the design of a 5-bit 2G/s flash ADC in a 65nm CMOS process. All simulations are on the transistor level with Spectre as the simulator in Cadence. For a 5-bit target, the mismatch effect is relaxed to some extents. Thus, a low-power sizing approach with a larger W/L transistor ratio has been adopted. The simulated DNL and INL at 2GS/s for a full scale 200kHz sinewave signal are within +0.091/–0.071LSB [Fig. 8(a)] and +0.066/–0.062LSB [Fig. 8(b)], respectively. The output spectrum of the ADC with a 31.6MHz (2511.1MHz) sine input is plotted in Fig. 9(a) [Fig. 9(b)], where the key performance metrics are shown. The dynamic performances of the ADC at a 2-GS/s sampling frequency (F_s) without [Fig. 10(a)] and with [Fig. 10(b)] reset switches are plotted as a function of input frequency (F_{in}). Without the reset switches, the (SFDR, SNDR, ENOB) is (32.55dB, 28.65dB, 4.47 bits) at 31.6MHz F_{in}, and (27.35dB, 25.75dB, 3.99 bits) at 510.1MHz F_{in}, limited by the 3rd harmonic in the output spectrum. The nonlinearity effects also

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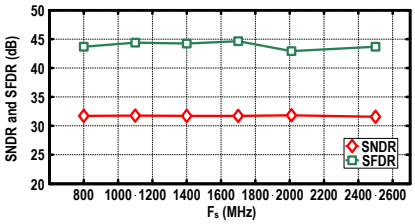
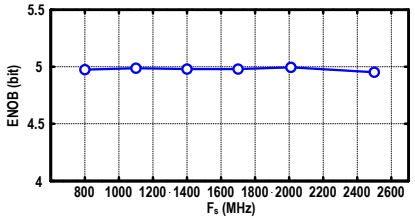
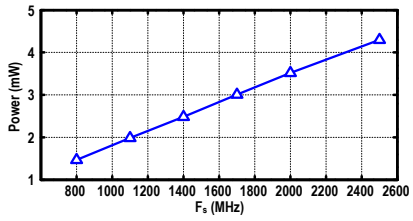


(a)

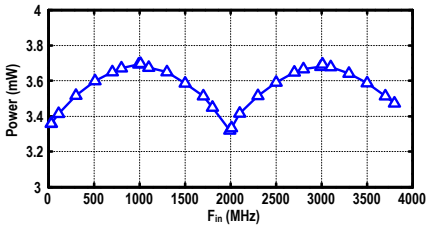


(b)

Fig. 11. Simulated (a) SNDR and SFDR and (b) ENOB versus F_s. The input signal frequency is 249.1MHz.



(a)



(b)

Fig. 12. Simulated power consumption versus (a) F_s under a full-scale input signal at 249.1MHz, and (b) F_{in} under a 2GHz sampling frequency.

become more pronounced at higher F_{in}. Differently, with the reset switch applied at every sampling cycle, the memory effect can be solved, thereby a better linearity. Simulation results show that the (SFDR, SNDR, ENOB) are improved to (44.45dB, 31.83dB, 4.99 bits) at 31.6-MHz F_{in}, and (44.2dB, 31.81dB, 4.99 bits) at 510.1MHz F_{in}, thanks to the reset switches help eliminating the 3rd harmonic.

At 249.1MHz F_{in}, the dynamic performances of the ADC as a function of F_s are shown in Fig.11(a) and (b). The ENOB is still 4.52 bits up to a 3411.1MHz F_{in}, and the SFDR is minimally 33 dB. Over a wide input bandwidth of 1301.1MHz (beyond the Nyquist), the ADC still achieves 4.92-bit ENOB and 41.0-dB SFDR. The ERBW (frequency at which the ENOB drops by 0.5dB) is up to 3.6GHz.

The power consumption varies with F_s [Fig. 12(a)] and F_{in} [Fig. 12(b)]. For instance, with a full-swing input signal at 249.1 MHz, the power is 1.53mW (4.09mW) at a F_s of 0.8GS/s (2.5GS/s). The relationship is wide-range linear. Thanks to the proposed split-ROM encoder, the ADC can convert an input signal up to 3.6GHz that covers almost 4 Nyquist bands. At the first Nyquist (0 to 1GHz), the power increases with F_{in} as expected. Interestingly, since the sampling operation is symmetrical, the power in the second Nyquist (1 to 2GHz) is also symmetrical to the first one, and such a power waveform repeats in the third and fourth Nyquist domains close to 4GHz.

VI. Conclusions

Two circuit techniques for very-high-speed flash ADCs have been proposed. The first is a calibration-intensive dynamic comparator. It alleviates the issue of kickback noise by modifying the built-in reference voltage generation in the source node of the input transistor pair. There is also a proper reset function for cleaning the memory effect due to the dielectric relaxation in the capacitors, showing better static and dynamic linearity performances. Another technique is the split-ROM encoder for halving the signaling path, effectively alleviating the parasitic effects. Both techniques were combined in the design of a 5-bit flash ADC in 65nm CMOS. With 3.69mW of power, the ADC operated at 2GS/s shows a simulated ENOB of >4.5 bit up to a 3.6GHz ERBW. The DNL and INL are within +0.091/–0.071LSB and +0.066/–0.062LSB, respectively.

Acknowledgement

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