A 89fJ-FOM 6-bit 3.4GS/s Flash ADC with 4x Time-Domain Interpolation

Jianwei Liu[1], Chi-Hang Chan[1], Sai-Weng Sin[1], Seng-Pan U[1, 2], Rui Paulo Martins[1, 3]
1 – State-Key Laboratory of Analog and Mixed Signal VLSI
Dept. of ECE, Faculty of Science and Technology, University of Macau, Macao, China
2 – Also with Synopsys Macau Ltd.
3 – On leave from Instituto Superior Técnico/Universidade de Lisboa, Portugal
email: ivorchan@ieee.org

Abstract - **This paper presents a 6-bit 3.4 GS/s flash ADC in 65 nm CMOS. The proposed 4x time-domain interpolation technique allows the reduction of the number of comparators from the conventional 63 to 16 in a 6-bit flash ADC. Without extra clocking and calibration in the interpolated stage, the proposed scheme effectively achieves a 4x interpolation factor with simple SR-latches. Offset calibration is only applied to the comparators and implemented on-chip. Measurement results show that the prototype can achieve 3.4 GS/s with a total power consumption of 12.6 mW at 1 V supply. Besides, it exhibits a 34.2 dB SNDR at Nyquist, which yields a Walden FoM of 89 fJ/conversion-step.**

I. INTRODUCTION

Next generation communication systems demand low-power and high-speed, up to several gigasample-per-second ADCs. The flash ADC is known as the fastest single channel ADC architecture which relies on the parallelism operation of the comparators. However, its number of comparator grows exponentially with the bit resolution leading to a large area overhead. Besides, the usage of this power dissipation is also not efficient because only a single comparator is critical at each conversion whereas the rest are just dissipating power to obtain a trivial answer. While time-interleaved and multi-bit SAR architectures have shown good energy efficiency [1] in this range of specifications, they usually require a complicated calibration scheme or higher design complexity leading to a larger core area.

Thanks to the technology scaling, offset calibrations can be integrated on-chip, thus often allowing the removal of the static pre-amplifier in the comparators on the conventional architecture. Then, with only dynamic power consumption, single channel flash ADCs are able to achieve as low as 59.3 fJ/conv.-step FoM at 5 GS/s with advanced technology nodes (32nm SOI) [2]. Besides, many different works [3][4] try to utilize the time information from the dynamic comparator's output to perform the folding or interpolation with only dynamic power consumption. These works also achieve very competitive FoMs in a single channel designs.

This paper presents a flash ADC that needs only 16 dynamic comparators and 45 SR-latches to achieve 6-bit resolution. With only dynamic power consumption, this ADC has an interpolation factor of 4. The interpolated SR-latches do not require extra calibration or clock control; therefore, the design complexity is low. Furthermore, the input capacitance and the power of the clock buffers are also reduced due to a smaller number of comparators. The experimental results of a 65 nm CMOS prototype demonstrate the effectiveness of the proposed interpolation technique. The power consumption is 12.6 mW at 3.4 GS/s and achieving 34.2 dB SNDR at Nyquist.

This research work was financially supported by Research Grants of University of Macau and Macao Science & Technology Development Fund (FDCT) under FDCT/055/2012/A2.

II. ADC ARCHITECTURE

Fig. 1 demonstrates the architecture of the proposed 4x time-domain interpolation flash ADC. For simplicity, the architecture is described in a single-ended version. The ADC mainly consists of a bootstrapped-switch sampling front-end, a reference ladder for reference generation, 16 dynamic comparators (CMP), 45 SR-latches which interpolated between every two adjacent CMPs' output, digital encoder and a digital offset calibration circuit for the dynamic comparators. In the comparison phase, the CMPs compare the sampled signal with

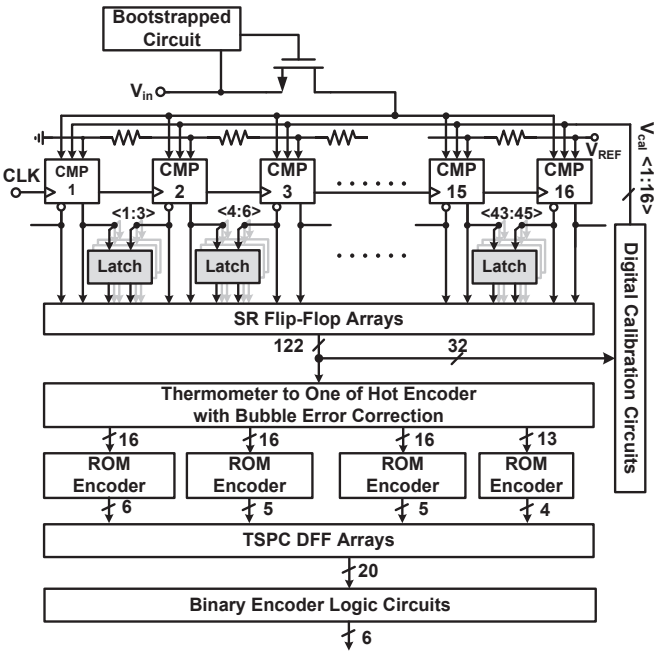

Fig.1. Overall ADC architecture.

978-1-4673-7191-9/15/$31.00 ©2015 IEEE

their corresponding reference voltages and then the interpolated SR-latches compare the time difference from every two adjacent CMPs' outputs. In the end, the obtained 61 bits thermometer codes (from both CMPs and SR-latches) are stored and encoded in a four-sectioned ROM-based encoder [5]. Their outputs are then further decoded by the binary decoder logic circuits. With the interpolation, the number of comparator in the proposed architecture is reduced to only 16 for 6-bit from the conventional flash ADC design.

III. Review of Time-Domain Interpolation

Unlike the conventional interpolation scheme which adopts the information in the voltage domain at the static preamplifiers' outputs, the latch interpolation [3] utilizes the time information to achieve the same purpose. Fig. 2 (a) and (b) shows the setup of the conventional and the latch interpolation method with 2x interpolating factor, respectively. The conventional one consists of preamplifiers follow by clocked latches, while the latch interpolation just includes clocked latches along with other latches. Assumed the interpolating decision thresholds are at $V_{ref,N}$, both methods can generate this threshold by utilizing the adjacent (N+1 and N-1) outputs of the latches/preamplifiers. After applied these methods, one latch/preamplifier and a reference level can be saved. Since the clocked latch consists of a regeneration circuit at its output, the output is not linearly dependent on the input difference as the preamplifier. Instead, it can be considered as an exponential gain block with the following input-output relationship:

$$V_{out} = V_{in} \exp\left(\frac{T_{comp}}{\tau_{reg}}\right), \tau_{reg} = \frac{C_L}{g_m} \quad (1)$$

where V_{out} is the output voltage of the latch, V_{in} is the initial output voltage at the beginning of the latching phase, g_m is the transconductance of the inverter that incorporates of the latch, T_{comp} is time given for the regeneration and C_L is the load capacitance. From (1), it can be found that linear interpolation from the latch's outputs is not possible as the output eventually will reach supply or ground; however, the input information is still propagating to the output in a different form. This can be illustrated by (2) when considering the time required for the comparator to regenerate to a valid-logic-level (V_{vaild}).

$$t_{comp} = \tau_{reg} \cdot \ln\left(\frac{V_{valid}}{V_{in}}\right) \quad (2)$$

From (2), it can be found the regeneration time depends on the input difference (V_{in}). Even though this time (delay) is not linearly dependent with the input, the time information is possible to extract for extra bit(s) information.

As the interpolating elements changed from the static preamplifier to the latch, the design benefits from its low and dynamic power characteristic, and achieves power effective interpolation. Based on the above interpolation concept, this work extends and accomplishes a 4x interpolation factor with little overhead which will be introduced in detail in the next section.

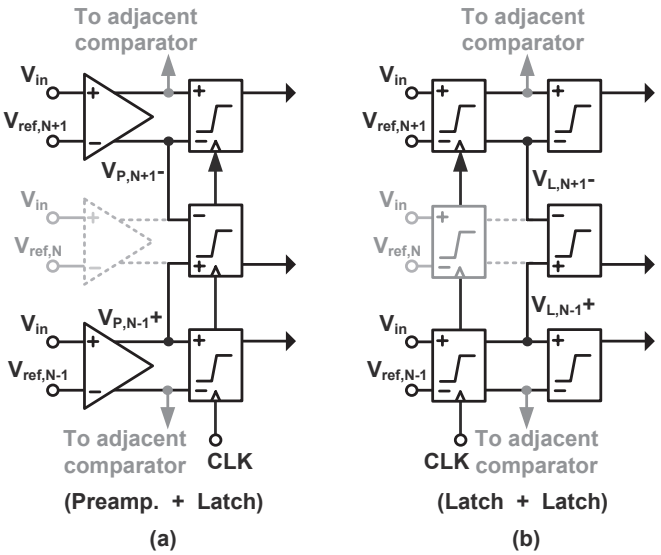

Fig.2. 2x interpolation (a) voltage domain; (b) time domain

IV. Proposed 4x Time-Domain Interpolation

Fig. 3 shows a detailed configuration of the proposed 4x time-domain latch interpolation technique (one unit). It consists of two stages where the 1st stage includes two comparators and the 2nd stage has three interpolating SR-latches. The 1st stage comparators (CMP_1 and CMP_2) compare the input signal (V_{in}) with their corresponding reference voltages ($V_{REF}[k-2]$ / $V_{REF}[k+2]$). Noted that three comparators are removed between CMP_1 and CMP_2, which are supposed to have their reference voltages as: $V_{REF}[k-1]$, $V_{REF}[k]$ and $V_{REF}[k+1]$. Instead, the decisions of these reference voltages are given in the SR-latches in the 2nd stage. There are totally 3 SR-latches in the 2nd stage and only two with deliberately built-in time offset (1 and 3). These 3 SR-latches compare the time difference at the neighboring comparator's outputs (QB_2 and Q_1) which generates extra three decisions for reference voltages at $V_{REF}[k-1]$, $V_{REF}[k]$ and $V_{REF}[k+1]$, as shown in Fig. 4. Equivalently, the time offset in $Latch_2$ (Fig. 3) is zero corresponding to $V_{REF}[k]$ while the remaining two are shifted by ±δt corresponding to $V_{REF}[k\pm1]$.

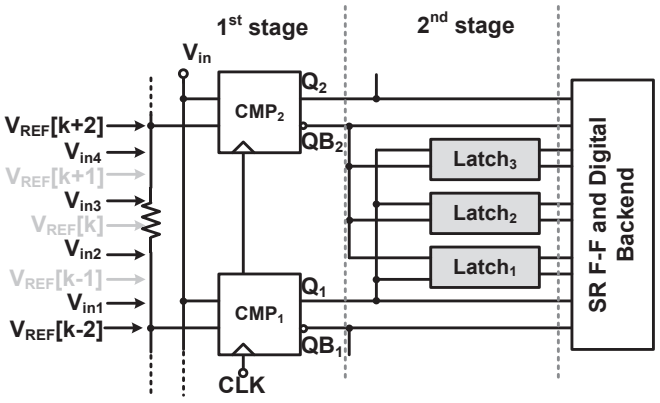

Fig.3. Proposed architecture 4x time-domain latch interpolation

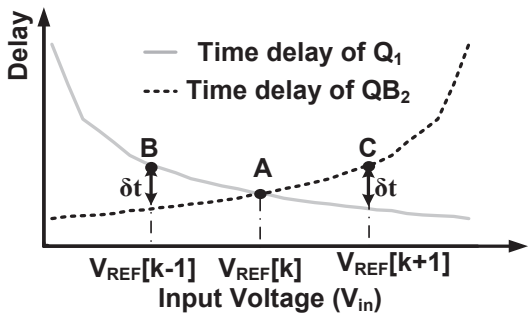

Fig.4. Extra decision reference with time offset.

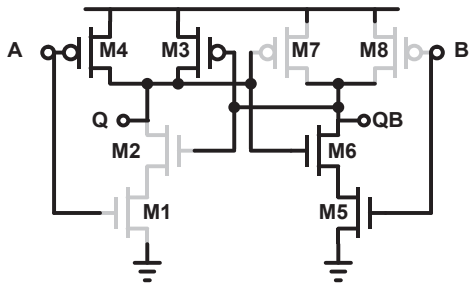

Fig.5. Circuit schematic of the adopted SR-latch

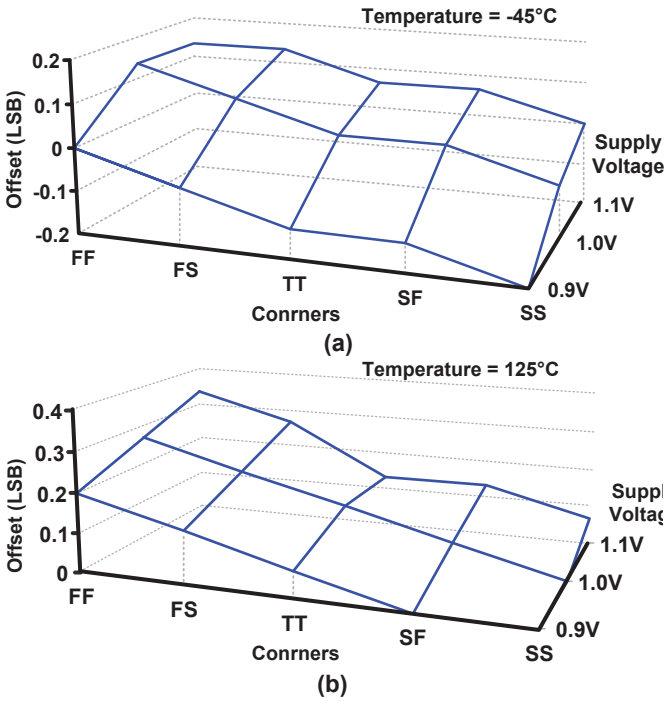

Fig.6: Simulated input-referred reference-voltage-variation of the size-weighted latch under the PVT (a) -45˚C (b) 125 ˚C.

The architecture of the 1st stage comparators is StrongArm [6] with extra input pair for calibrating its offset voltage. The calibration procedure is similar as [7]. The latches in the 2nd stage are simply the conventional NAND-based SR-Latch as show in Fig. 5. When the circuit is in fully symmetrical setup, it has a zero-crossing with time difference at zero. On the other hand, deliberated mismatch (time offset) can be inserted to this latch by unbalance the width of the transistors. For instance, by reducing the width of M3, M4, M5 and M6, and enlarging M1, M2, M7 and M8, a positive time offset can be accomplished. Similarly, the negative time offset can be obtained simply by swapping the inputs (A & B). Even though these time offsets are realized by size-weighted, their variation under PVT has similar trend as the delay of the comparator. This can be verified by the simulation results provided in Fig. 6. The results are obtained from the interpolated latch at the boundary reference (worse-case in this design) with post-layout simulation in *Spice* level with the size adopted in this design. The results show the variation under different corners with 125°C and -45°C as well as 10% supply voltage variation. The effect on the time offset-drifted due to PVT is only within ±0.5 LSB. Besides, offset induced by device mismatch is also fairly small. According to the mismatch monte-carlo simulation results, the maximum variation is within 3σ = 0.4 LSB under all corners. This is also because the offset requirement in the 2nd stage is relax by half due to the interpolation [3].

V. Measurement Results

The proposed 6-bit flash ADC was fabricated in a 65 nm 1P7M digital CMOS process. Fig. 7 shows the die microphotograph; the active area is 0.034 mm^2 where on-chip offset calibration circuits occupy 0.025 mm^2. The ADC has a full-scale input range of 0.8 V_{pp} differential and an input capacitance of only 120 fF including parasitics. Fig. 8 illustrates the measured FFT plotted at near Nyquist input frequency with on-chip offset calibration. The SNDR before calibration is 18.6 dB and after calibration is improved to 34.2 dB. At high input frequency, the 3rd harmonic limits the SFDR which is due to the sampling nonlinearity and edging effect of the boundary comparators. Fig. 9 shows the measured dynamic performance across different sampling frequencies with low frequency input. It can be seen that the prototype maintains a constant SNDR in a wide range of sampling frequencies. Fig. 10 shows the measured dynamic performances across different input frequencies at 3.4 GS/s. The SNDR remained above 32 dB until an 1.8 GHz input. Fig. 11 shows the measured static performance. The on-chip offset calibration improves DNL from 3.75/-1 LSB to 0.48/-0.37 LSB and the INL from 4.21/-6.34 LSBs to 0.64/-0.48 LSBs. Fig. 12 compares this design with all state-of-the-art ADCs from ISSCC and VLSI conferences [8] with sampling frequencies larger than 2 GHz. For single channel designs, the proposed ADC only has a higher FoM than one circuit in 32nm SOI. Table I summarizes and compares the overall measured performance with state-of-the-art flash ADCs. The total power consumption is 12.6 mW, at 3.4 GS/s from 1 V supply, where the analog and digital blocks consume 9.1 mW and 3.5 mW, respectively. This work exhibits an excellent FoM of 89 fJ/conv.-step @Nyquist for the high-speed single channel flash ADC.

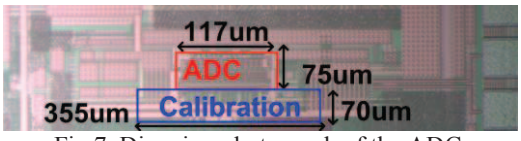

Fig.7. Die microphotograph of the ADC.

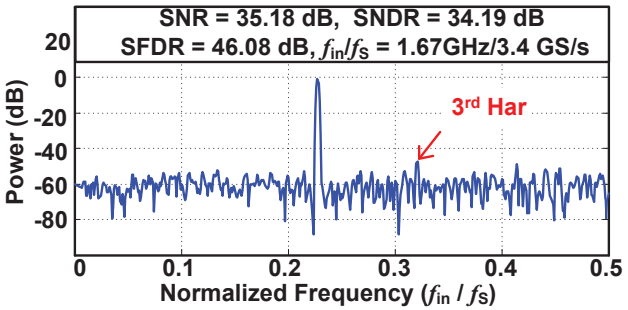

Fig.8: Measured FFT of the digital output (decimated by125)

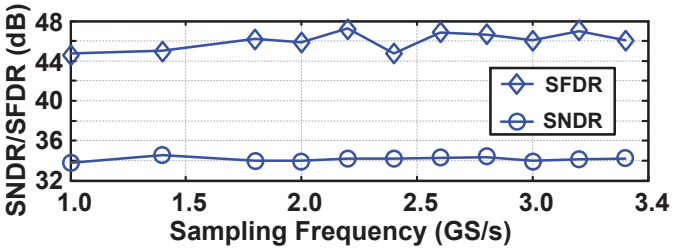

Fig.9. Measured SFDR/ SNDR v.s. sampling frequencies.

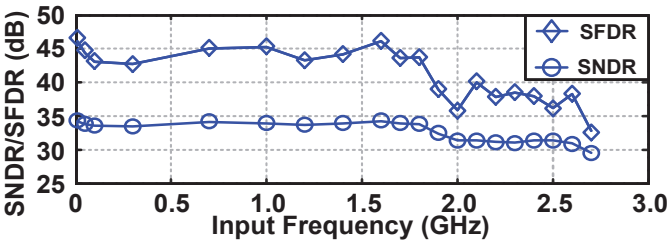

Fig.10. Measured SNDR/SFDR vs. input frequencies.

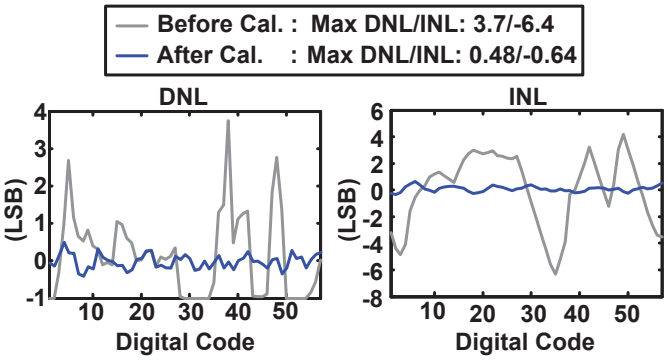

Fig.11: Measured static performance w/o & w/ calibration.

VI. Conclusions

A 4x time-domain latch interpolation technique is proposed which can reduce the number of dynamic comparators by 4-fold in conventional flash ADCs with only dynamic power consumption. By utilizing the time difference between two neighboring dynamic comparators, the interpolation technique shows a moderate level of tolerance on the PVT variation, with satisfactory measured performance from verified silicon results.

References

[1] C-H. Chan, et Al., "A 5.5mW 6b 5GS/S 4×-Interleaved 3b/cycle SAR ADC in 65nm CMOS," *ISSCC Dig. Tech. Papers*, pp. 1-3, Feb. 2015.

[2] V. H. -C. Chen et Al.,, "An 8.5mW 5GS/s 6b Flash ADC with Dynamic Offset Calibration in 32nm CMOS SOI," *Symp. VLSI Circuits*, pp. 264-265, Jun. 2013.

[3] Y. -S Shu, "A 6b 3GS/s 11mW Fully Dynamic ADC in 40nm CMOS with Reduced Number of comparators," *Symp. VLSI Circuits*, pp. 26-27, Jun. 2012.

[4] Miyahara, M., et Al., "22.6 A 2.2GS/s 7b 27.4mW time-based folding-flash ADC with resistively averaged voltage-to-time amplifiers"," *ISSCC Dig. Tech. Papers*, pp. 399-389, Feb. 2014.

[5] K. Deguchi., et Al., "A 6-bit 3.5GS/s 0.9-V 98-mW flash ADC in 90 nm CMOS," IEEE *J. Solid-State Circuits*, vol. 43, no. 10, pp. 2303–2310, Oct. 2008.

[6] B.Wicht., et Al., "Yield and speed optimization of a latch-type voltage sense amplifier," IEEE *J. Solid-State Circuits*, vol. 39, no. 7, pp. 1148–1158, Jul. 2004.

[7] C-H. Chan, et Al., "A 5-Bit 1.25-GS/s 4x-Capacitive-Folding Flash ADC in 65-nm CMOS," IEEE *J. Solid-State Circuits*, vol. 48, nol. 9, pp 2154,2169, Sep. 2013

[8] B. Murmann, "ADC Performance Survey 1997-2015," [Online]. Available: http://web.stanford.edu/~murmann/adcsurvey.html.

[9] J.-I. Kim, et Al., "A 6-b 4.1GS/s Flash ADC With Time-Domain Latch Interpolation in 90-nm CMOS," IEEE *J. Solid-State Circuits*, vol. 48, nol. 6, pp1429-1441, Jun. 2013

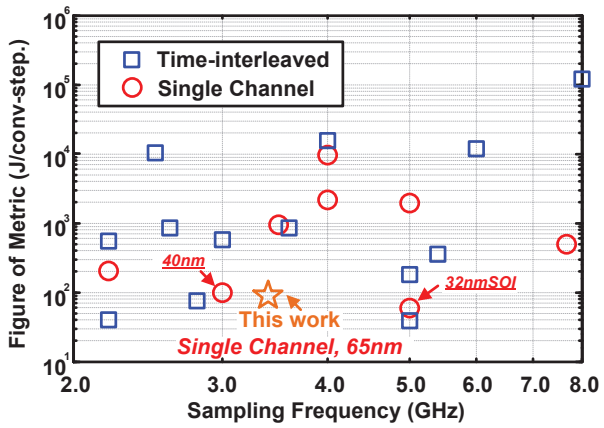

Fig.12. FoM for previously reported >2GS/s in ISSCC and VLSI and this work

Table I Summary of performance and benchmark with state-of-the-art

	[4]	[3]	[9]	[2]	This work
Architecture	Flash	Flash	Flash	Flash	Flash
Resolution (bit)	7	6	6	6	6
Technology (nm)	40	40	90	32 SOI	65
Sampling Rate (GS/s)	2.2	3	4.1	5	3.4
Supply Voltage (V)	1.1	1.1	1.2	0.85	1.0
Power (mW)	27.4	11	76	8.5	12.6
ENOB @Nyquist	5.92	5.21	5.05	4.85	5.39
Area (mm^2)	0.052	0.021	-	0.02	0.034
Input capacitor (fF)	200	72	-	135	120
Offset Calibration	No need	On chip	On chip	On chip	On chip
FoM @Nyq (fJ/conv.step)	210	100	625	59.6	89