Sub-threshold VLSI Logic Family Exploiting Unbalanced Pull-up/down Network, Logical Effort and Inverse-Narrow-Width Techniques

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Abstract – This paper presents a complete energy optimized sub-threshold standard cell library exploiting unbalanced pull-up/down (PU/PD) network, logical effort and inverse-narrow-width (INW) techniques. Individual logic cell is optimized for ultra-low-energy applications with low-to-moderate speed requirement. Three 14-tap 8-bit FIR filters are fabricated using a 0.18-µm CMOS technology, while one of them achieved the minimum energy/tap (0.0234 pJ) and 0.365 Figure-of-Merit (FoM) at 100 kHz, 0.31 V.

I. Introduction

Recent emerging applications including wireless sensor nodes and wearable/implantable biomedical systems require low-to-moderate computations and stringent power budget due to the limited battery capacity. As a result, power efficient designs are of utmost importance for a prolonged system lifespan. Sub-threshold operation offers the opportunity for integrated digital circuits to achieve high energy efficiency. It has been demonstrated in [1] that minimum energy consumption is achieved when logic cells are operating in the sub-threshold regime. This work exploits the unbalanced PU/PD network, logical effort and INW to further improve the individual cell performance [2].

II. Energy-Efficient Logic Family Design

Typically, a balanced pull-up and pull-down network approach is achieved by increasing the PMOS size or stacking the NMOS devices for comparable driving capability and hence the improved SNM (static noise margin). Nevertheless, this will increase the effective capacitance and width that result in sub-optimal energy efficiency with reduced operating speed. Fig. 1 shows the minimum threshold voltages considering the inverse-narrow-width effect with a supply voltage of 0.3 V. It can be observed that a minimum threshold voltage is achieved with a NMOS and PMOS width of 220 and 400-590 nm, respectively. Fig. 2 demonstrates the power-delay product (PDP) of a reference inverter, with better performance achieved using an unbalanced PU/PD network.

Fig. 3 illustrates the use of logical effort by modelling transistors with equivalent resistors, and the dimension of a stacked/parallel device is scaled to maintain an identical total resistance as the reference inverter. Fig. 4 shows the PDP improvement of the NAND3 and NOR3 gates using the unbalanced PU/PD network and logical effort techniques.

Due to the reduced logical effort for improved speed and robustness, the transmission-gate based design is selected for composite gate designs. Fig. 5 shows the conventional and transmission-gate based XNOR gate implementation. It should be noted that the architecture with smaller logical effort largely reduce the intrinsic capacitive load and the number of transistors, both of which can lower the energy consumption. Fig. 6 shows the Monte Carlo simulations of NAND3/NOR3 which exhibit the most stringent PD/PU delays in the logic family. It can be observed that both gates achieve operating speed (>500 kHz) suitable for biomedical applications with a low-to-moderate frequency requirement.

III. Measurement Results

To validate the practicability of the sub-threshold logic family, three FIR filters optimized for 0.3 V, 0.45 V and 0.6 V supply are fabricated in a 0.18-µm CMOS technology. Fig. 7 shows the chip micrograph of the three implementations, with active areas of 0.1155, 0.053 and 0.049 mm^2, respectively. Fig. 8 illustrates the testing setup for the FIR filters. Table I shows that the 0.45 V and 0.6 V FIR filters achieved FoMs of 0.365 and 0.4632 at 100 kHz, respectively, which are well comparable to the state of the art [3-5].

IV. Summary and Conclusions

This paper proposes a practical design methodology of sub-threshold logic family exploiting unbalanced PU/PD network, logical effort and INW techniques. Measurement results show that the 0.45 V and 0.6 V FIR filters implemented using a 0.18-µm CMOS technology achieve FoMs of 0.365 (0.31 V) and 0.4632 (0.39 V) at 100 kHz.

Acknowledgements

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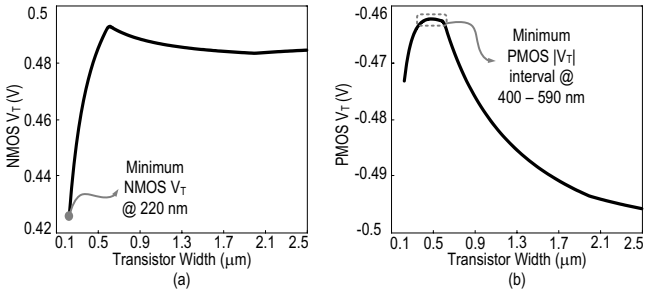

Fig. 1. (a) NMOS, (b) PMOS V_T vs. transistor width, at V_{DD} = 0.3 V.

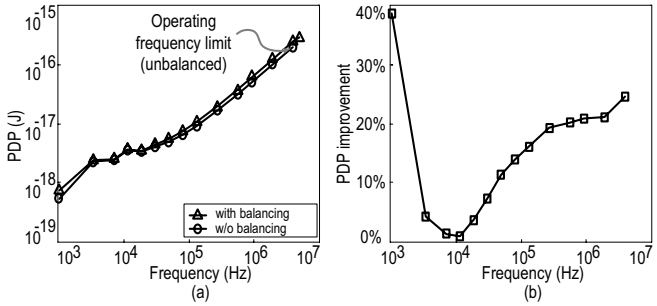

Fig. 2. (a) PDP, and (b) PDP improvement of a reference inverter (FO4 loading) with balanced (P/N ratio = 5/1) and unbalanced (P/N ratio = 2/1) Pull-up/down network vs. operating frequency at 0.3 V.

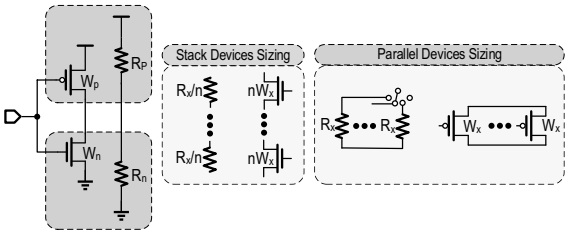

Fig. 3. Resistance model of the reference inverter, and the sizing methodology of stack/parallel devices.

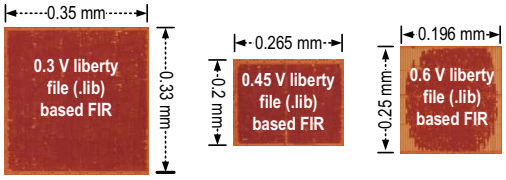

Fig. 7. Die micrographs of the FIR test chips.

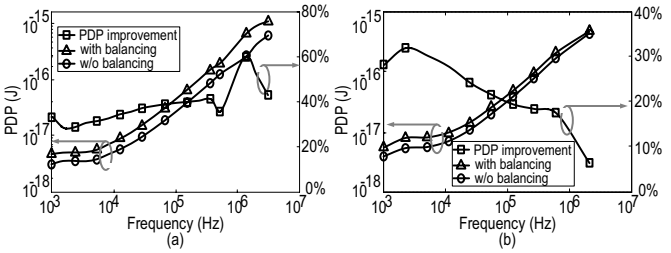

Fig. 4. Power-delay product of (a) NAND3; (b) NOR3 with balanced (P/N ratio = 5/1) and unbalanced (P/N = 2/1) Pull-up/down network vs. operating frequency @ 0.3 V.

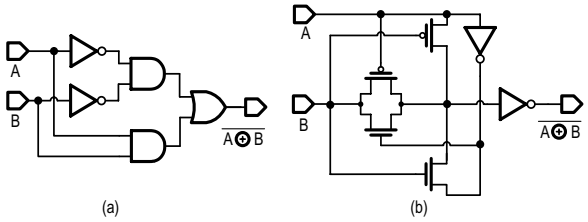

Fig. 5. XNOR gate (a) conventional; (b) transmission-gate based.

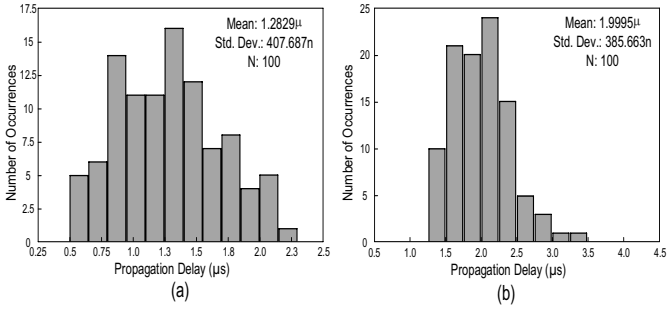

Fig. 6. 100 times Monte-Carlo simulation of (a) NAND3; (b) NOR3 for delay characterization @ 0.3 V.

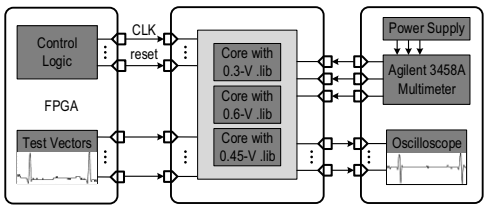

Fig. 8. Test setup for the FIR filters.

TABLE I.
COMPARISON OF FIR FILTERS DESIGNED USING SUB-THRESHOLD TECHNIQUE

	This Work				[3] JSSC'10	[4] JSSC'10	[5] TCAS-II'12
	with 0.45-V .lib		with 0.6-V .lib				
FIR Type	14-tap, 8-bit				14-tap, 8-bit	8-tap, 8-bit	30-tap, 8-bit
Technology	0.18-μm				0.13-μm	90-nm	0.13-μm
Optimum V_{DD} (V)	0.31		0.39		0.27	0.29	0.35
Frequency (Hz)	100k		100k		20M	148k	29k
Energy/Tap (pJ)	**0.02735**	**0.0234**	**0.03568**	**0.02964**	1.11	0.6275	1.1
Power (nW)	**38.29#**	**32.7**	**49.95#**	**41.5**	310,000	742.96	32
FoM*	**0.4273**	**0.3650**	**0.5575**	**0.4632**	17.37	9.80	0.57
Area/Channel (mm^2)	0.053		0.049		0.38	N/A	0.058

*FIR FoM = power(nW)/freq.(MHz)/# of taps/input bit length/coefficient bit length.
#Multi-chip measurement results (mean value) from 15 chips.