A Digital PWM Controlled KY Step-Up Converter Based on Frequency Domain ΣΔ ADC

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***Abstract*—This paper introduces a digital PWM control of the KY step-up converter based on frequency domain sigma-delta (ΣΔ) analog-to-digital converter (ADC), in which we deduce the mathematical modeling of the KY step-up converter and the frequency-domain digitization technique based on the first-order non-feedback sigma-delta frequency discriminators (NF-SDFD). Then, the digital control of the KY converter with voltage control oscillator (VCO), NF-SDFD, cascaded integrator comb (CIC) decimator, PID compensator and digital pulse width modulation (DPWM) generator has been successfully built in MATLAB Simulink for verification. This modeling work is useful in the design of a low power digital controlled KY step-up converter with low output voltage ripple and fast transient response.**

Keywords—Frequency domain sigma-delta ADC; KY converter; Digital control.

I. INTRODUCTION

In the modern society, DC-DC converters are widely used in portable electronic devices such as: mobile phones, laptops and digital still cameras (DSC), etc. in order to convert the battery voltage into different voltage domains. The digital control of DC-DC converters leads to considerable benefits in terms of low power consumption, more flexibility to be re-configured, low sensitivity to process and temperature variations; immunity to noise and component aging and low quiescent current [1]. However, the digital controller for DC-DC converter always suffers from the accuracy issue due to the resolution of the analog-to-digital converter (ADC).

For power supply applications using low voltage battery, in most instances, it is necessary an uplift from low voltage to high voltage, thus a boost converter is usually applied, but with a pulsating output current leading to a large voltage ripple [2]. Moreover, the boost converter consists of a right hand plane zero, which deteriorates the converter stability and transient response performances. Recently, a voltage-boosting converter has been proposed, named as KY converter. When this converter is operating in continuous conduction mode (CCM), it has a lot of advantages such as non-pulsating current, low output ripple, and good load transient response [2], [3], which can eliminate the problems exhibited by the boost converter.

Conventionally, the analog closed-loop controller is usually applied to the DC-DC converters. But the analog controller suffers from high power consumption, it is sensitive to noise and parameters variations due to PVT, etc. In this paper, the analog controller will be replaced by a digital controller to overcome the above mentioned problems. The digital controller requires an A/D converter where the most adequate architecture would be the multi-bit flash A/D converter. However, the power consumption and the silicon area will be quite large if we use a multi-bit flash A/D converter [4]. In order to design a low power, with low sensitivity to noise and higher adaption flexibility to parameters variation, a frequency domain sigma-delta (ΣΔ) A/D converter [5], [6] can be applied, in which such architecture allows smaller area and lower quiescent power consumption when compared with the multi-bit flash and the conventional sigma-delta A/D converter.

At the present stage, the KY converter is applied on high power electronics area and the frequency domain sigma-delta ADC is utilized on lower power buck converter IC only. This paper combines the KY converter with the frequency domain sigma-delta ADC based on their advantages and successfully built a mathematical model for its behavior and characteristic study. This paper work aims to migrate the KY converter from power electronics area into integrated circuit (IC) design study with low power digital control, which has potential to substitute the conventional boost converter IC in some applications.

The advantages of this digital control method are low power, low sensitivity to noise, low output voltage ripple, wide ADC range resolution and higher flexibility to parameters variation. When compared with the conventional A/D converter, if the control circuit requires higher accuracy, the resolution of the NF-SDFD can be simply enhanced by increasing its sampling frequency instead of modifying the A/D converter design. In addition, the KY converter can reduce the output voltage ripple and improve the transient response in contrast with the boost converter [2].

The main contributions of this paper are:

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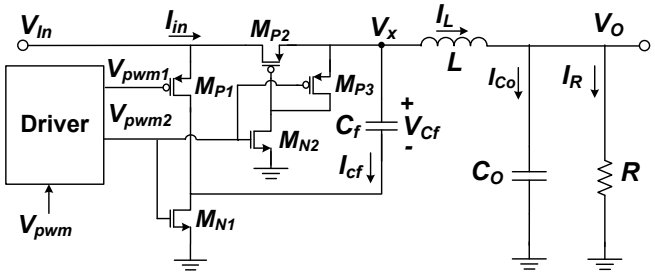
1. Combine the KY converter with the frequency domain ΣΔ ADC and provide an appropriate mathematical modeling and behavior study of this design.
2. Build up a circuit modeling for the digital controlled KY converter with NF-SDFD, cascaded integrator comb (CIC) decimator, PID compensator and digital pulse width modulation (DPWM) generator, necessary to predict the converter circuit performances before circuit integration.
3. Simulation verification and benchmark between the proposed digitally controlled KY converter with the low power passive ΣΔ modulator ADC [1] and the low power frequency domain ΣΔ ADC [5], [6].
4. This behavior model study can help for the digital controlled KY converter IC design in future.

II. Topology of the KY Step-Up Converter

Fig.1 shows the KY step-up DC-DC converter system which comprises a switched-capacitor charge pump converter and a buck converter combining the advantages of both [2], [3].



State 1: M_{P1} & M_{P3} are ON and M_{P2}, M_{N1} & M_{N2} are OFF
State 2: M_{P1} & M_{P3} are OFF and M_{P2}, M_{N1} & M_{N2} are ON

Fig. 1. KY step-up converter.

From Fig. 1, when M_{P1} and M_{P3} turn on and M_{P2}, M_{N1} and M_{N2} turn off the corresponding differential equations are:

$$L\frac{dI_L}{dt} = 2V_{in} - V_o \quad (1)$$

$$C_o\frac{dV_o}{dt} = I_L - \frac{V_o}{R} \quad (2)$$

$$I_{in} = I_L \quad (3)$$

On the other hand, when M_{P1} and M_{P3} turn off and M_{P2}, M_{N1} and M_{N2} turn on the equations will become:

$$L\frac{dI_L}{dt} = V_{in} - V_o \quad (4)$$

$$C_o\frac{dV_o}{dt} = I_L - \frac{V_o}{R} \quad (5)$$

$$I_{in} = I_L + I_{cf} \quad (6)$$

Based on (1) – (6), the simulink model of the KY converter can be built as shown in Fig. 2.

III. KY Step-Up Converter with Frequency Domain ΣΔ ADC

Fig. 3 depicts the proposed KY converter, which uses on the control loop a VCO based ΣΔ ADC. As Fig. 3 shows, the KY converter output voltage Vo is the input of a voltage control oscillator (VCO). The output of the VCO, running at the frequency f(t), is one the input the NF-SDFD circuit. It is processed together with the reference clock, f_{ck} to obtain a 1-bit stream signal similar to the one of a conventional first order sigma-delta modulator. The CIC decimator decimates the bit stream. Then the difference or error (e) between the Then, the error difference (e) between the digital reference and the decimated signal will be presented to the PID compensator which calculates the required duty cycle to set the output voltage at a desired value. Finally, the DPWM converts this duty cycle signal into a driver signal to control the KY converter power switches [5].

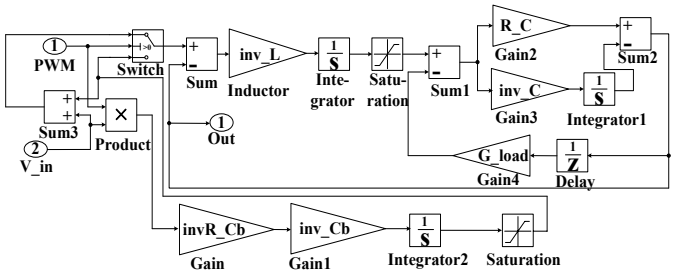


Fig. 2. Simulink model of the KY converter.

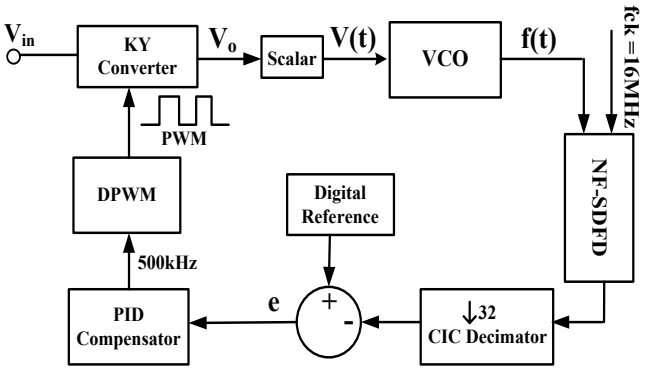


Fig. 3. KY converter based on the frequency domain ΣΔ ADC.

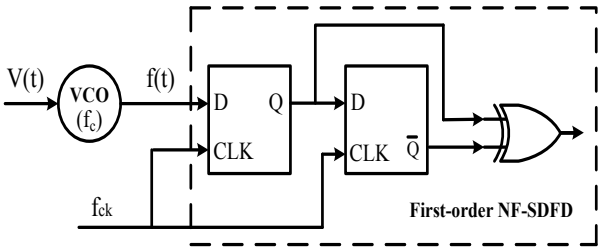


Fig. 4. A first-order NF-SDFD.

Fig. 4 shows the first-order NF-SDFD that consists of 2 D-type flip flop (DFF) and a digital differentiator gate (XOR). It digitizes the instantaneous frequency f(t) from its carrier frequency fc with high pass quantization noise shaping similar to the conventional sigma-delta ADC that digitizes the amplitude of input signals [7].

IV. Simulation Model and Results

A MATLAB Simulink simulations verifies the operation of the KY converter driven by the frequency domain ΣΔ ADC. Fig. 5 illustrates the built Simulink model. As shown the behavioral circuit uses the similar blocks as described in [6].

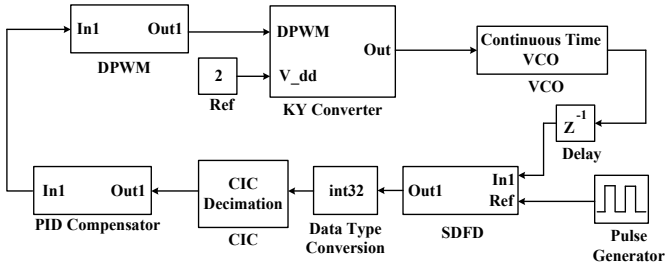


Fig. 5. Simulink model of the KY converter based on the frequency domain ΣΔ ADC.

The model of Fig. 5 consists of 6 main functional blocks, where the first is the KY step-up voltage regulator, the second is the VCO obtained from the Simulink library. The NF-SDFD transforms the analog signal into digital and a two-stage CIC decimator block uses a 16MHz sampling frequency. The PID compensator (with design similar to the analog controller) block converts the digital signal into a duty-cycle signal to achieve 60 degrees of phase margin, thus, it can maintain a good stability in the converter with a fast transient response. Finally, the DPWM generator contains a quantizer with the corresponding saturation model. In order to avoid the limit-cycle problem [8] the required resolution of the DPWM is defined as (7). Table I shows the design parameters used in the simulation. The main clock frequency f_{ck} is 16 MHz and the DPWM frequency is 500KHz.

$$n_{pwm} \geq \text{int}\left[n_{adc} + log_2\left(\frac{V_{ref}}{V_{max,adc} \times D}\right)\right] \qquad (7)$$

For (7), n_{pwm} is the PWM resolution, i.e. the number of output bits of the PWM. n_{adc} is the A/D converter resolution, i.e. the number of its output bits. V_{ref} is the reference voltage, $V_{max,adc}$ is the full-range voltage of the ADC, with the assumption of unipolar conversion in the range from 0 to $V_{max,adc}$ and D is the duty ratio of the KY converter.

Fig. 6 shows the subsystem of the first-order NF-SDFD. According to [7], in order to reduce the quantization error, using the sampling frequency higher than twice of the maximum VCO frequency, for example, $f_{ref} = f_{ck} \geq 2(f_c+\Delta f)$, the outcome from counting the VCO signal zero crossings will be restricted to zero and one. Then, the output of the VCO is an FM modulated signal with carrier frequency f_c =5MHz and Δf =20% of f_c. The input reference frequency $f_{ref} = f_{ck}$ is a 16MHz clock signal.

TABLE I. Design Parameters for Simulation

Parameter	Value	Parameter	Value
V_{in}	2 V	L	1 µH
C_o	80 µF	C_f	20 µF
V_o	3 V	I_o	0.6 A
R_o	5 Ω	f_{ck}	16 MHz
R_C_o (ESR of C_o)	0.1 Ω	R_ C_f (ESR of C_f)	0.1 Ω
R_L (ESR of L)	0.1 Ω	DPWM frequency	500 KHz

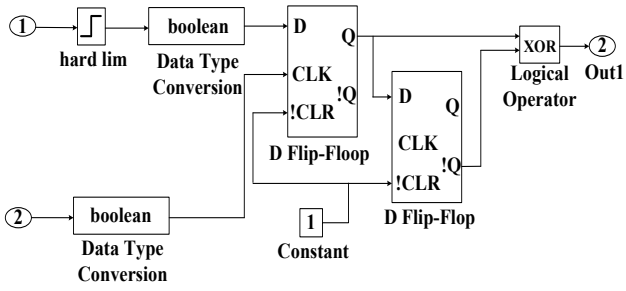


Fig. 6. Simulink model of the first-order NF-SDFD.

Fig. 7 shows the schematic of the 2-stage CIC decimator that can be obtained from the Simulink library. This decimator consists of an integrator and a comb filter. It transforms the digital input from short words occurring at high sampling rate to longer words at lower sampling rate closer to Nyquist rate. Here, we design the CIC decimator to achieve a sampling rate reduction of 32.

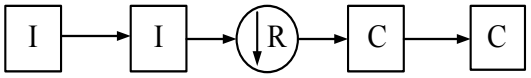


Fig. 7. Two-stage CIC decimator.

The transfer function of an N-stage CIC decimator is defined as (8) [9]:

$$\text{H(z)} = H_I(z) \cdot H_C(z) = \frac{(1-z^{-RM})^N}{(1-z^{-1})^N} = (\sum_{k=0}^{RM-1} z^{-k})^N \qquad (8)$$

For (8), N is the number stages, M is differential delay and usually it is equal to 1 or 2, R is the rate reduction factor. In this design, the values are N=2, M=1 and R=32.

Figs. 8 and Fig. 9 show the simulation results of the KY converter with the passive ΣΔ modulator ADC and the frequency domain ΣΔ ADC. Fig. 10 shows the corresponding V_o ripple simulation results, just only 1mV. Table II

summarizes their simulation results. When compared with the passive ΣΔ ADC model, the frequency domain ΣΔ ADC controlled KY converter can obtain lower overshoot, shorter settling time.

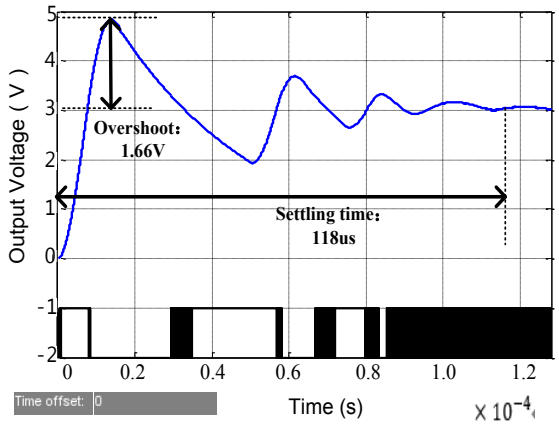


Fig. 8. Simulation result of the KY converter based on the passive ΣΔ modulator ADC.

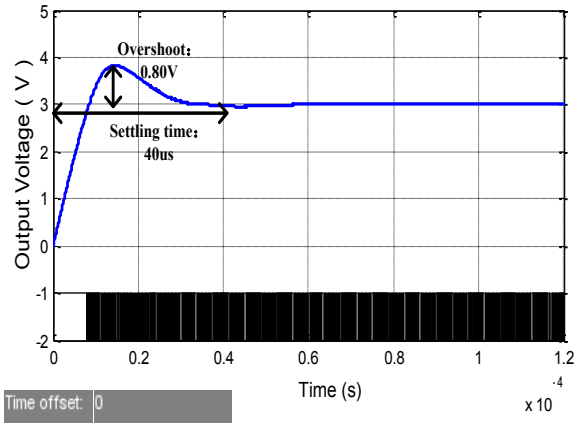


Fig. 9. Simulation result of the KY converter based on the frequency domain ΣΔ ADC.

(a)

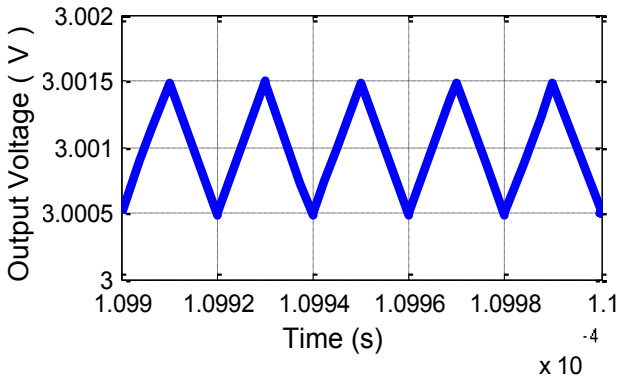


Fig. 10. Vo ripple of the KY converter based on the frequency domain ΣΔ ADC.

TABLE II. PERFORMANCE COMPARISON BETWEEN THE KY CONVERTER BASED ON THE PASSIVE ΣΔ MODULATOR AND THE FREQUENCY DOMAIN ΣΔ ADC

Parameter	Passive ΣΔ ADC Controlled KY Converter	Frequency Domain ΣΔ ADC Controlled KY Converter
Overshoot	1.66 V	0.80 V
Settling Time	118 μs	40 μs

V. CONCLUSIONS

This paper presents the mathematical and behavior model of the KY converter with frequency domain ΣΔ ADC. This digital control of the KY converter with VCO, NF-SDFD, CIC decimator, PID compensator and DPWM has been successfully built in MATLAB Simulink for verification purposes. This work allows the estimation and prediction of the KY converter output voltage ripple, overshoot, settling time and other system performances by using the low power frequency domain ΣΔ ADC. This behavior model study can help for the design of the digital controlled KY converter IC in future.

ACKNOWLEDGMENT

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