A 0.7 to 1 GHz Switched-LC N-Path LNA Resilient to FDD-LTE Self-Interference at ≥40 MHz Offset

Gengzhen Qi [#*], Barend van Liempd [*+], Pui-In Mak [#], Rui P. Martins [#%], Jan Craninckx [*]
[#] State Key Laboratory of Analog and Mixed-Signal VLSI and FST-ECE, University of Macau, Macau, China
[*] Perceptive Systems, imec, Leuven, Belgium
[+] ETRO Department, Vrije Universiteit Brussel, Brussels, Belgium
[%] On leave from Instituto Superior Técnico, Universidade de Lisboa, Portugal

***Abstract*—This paper proposes a self-interference-resilient LNA for the FDD-LTE covering 0.7 to 1GHz. It incorporates a switched-LC N-path network with gain-boosting and optimum-biasing techniques to enhance the out-of-band (OOB) linearity at ≥40MHz offset. Implemented in 0.18µm SOI CMOS, the LNA achieves >31.2dB output rejection, +26.2dBm (+8dBm) OOB-IIP$_3$ (iB$_{1dB}$) at ≥40MHz offset and 6.8dB blocker NF at +4dBm blocker power for the default mode, while consuming a reasonable power of 48.4 to 62.5mW. When reconfigured to high-rejection mode, the LNA offers a tunable cancellation notch improving the output rejection to >50dBc.**

***Index Terms*—LTE, FDD, wireless, communication, tunable filter, filter, low-noise amplifier, LNA, N-path, LO generator.**

I. Introduction

High-Q tunable filtering is crucial to enable tunable RF front-ends for frequency-division duplexing (FDD) operation in LTE Advanced and 5G. To support FDD, the RF front-end has to provide adequate isolation between the transmitter (TX) and receiver (RX) at two frequencies: 1) the TX frequency (f_{TX}) to prevent the high-power TX signal from causing gain compression of the RX's low-noise amplifier (LNA), and 2) the RX frequency (f_{RX}) to prevent the TX-generated noise in the RX band from de-sensitizing the RX chain. The key challenge posed by the FDD-LTE standard is that the TX-RX duplex spacing is as low as 40MHz, depending on the band. Existing products are based on surface-acoustic wave (SAW) duplexers to attain sufficient isolation at both frequencies (see Fig. 1(a)). Yet, as more and more bands are defined towards 5G, adding more SAW duplexers does not scale well and will significantly increase the form factor of the system.

Electrical-balance duplexers (EBDs) promise to replace many off-chip SAW duplexers (see Fig. 1(b)). They provide TX-RX isolation by *balancing* an antenna impedance Z_{ANT} with an on-chip balance network (Z_{BAL}). Yet, EBDs have limited isolation bandwidth (BW), inadequate to cover both f_{TX} and f_{RX}, or entail a highly complex balance network [1]. While the EBD can provide >50dB isolation at f_{RX}, the isolation at f_{TX} is degraded due to the frequency dependency of Z_{ANT}. Thus,

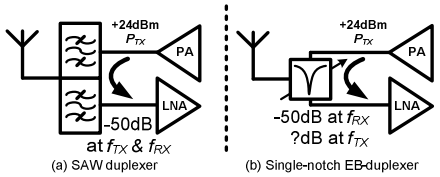

Fig. 1. (a) SAW duplexer isolates at both f_{RX} and f_{TX}; (b) Tunable RF front-end EBD, with limited isolation at f_{TX}.

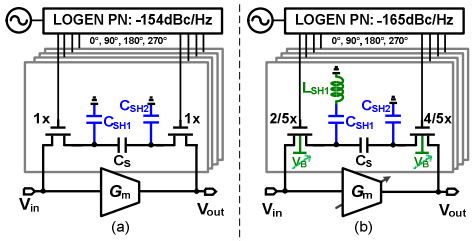

Fig. 2. (a) Switched-*C* [3] and (b) proposed switched-*LC* N-path LNA.

it is desired to develop an LNA that can cover many FDD-LTE bands, withstand the large TX signal, and be linear enough to handle the intermodulation between the TX self-interference and an out-of-band (OOB) jammer.

Fig. 2(a) depicts a blocker-resilient LNA that combines the gain-boosted N-path technique [2] with a linear class-A/B transconductance (G_m) and $C_{SH1,2}$ to enhance the OOB linearity and rejection [3]. Despite the high OOB rejection at the LNA's output, the optimal rejection is achieved at a ≥150MHz notch offset, too large for FDD applications.

This paper reports a self-interference LNA (Fig. 2(b)) that can cover the FDD-LTE low-bands, from 0.7 to 1GHz. The LNA can be integrated with an EBD using an RF SOI CMOS process suitable for large signal handling [1]. To achieve rejection at close-by frequencies we propose a switched-*LC* N-path feedforward network combined with gain-boosting and optimum-biasing techniques. Besides, a power-optimized low-noise LO generator (LOGEN) is employed to achieve -165dBc/Hz phase noise. The LNA achieves +26.2dBm OOB-IIP$_3$ and +9dBm OOB-iB$_{1dB}$, while consuming 48.4-62.5mW. NF only starts to increase for blockers >0dBm and is just 9.5dB even for +7dBm blocker.

II. Implementation Details

The proposed LNA features a class-A/B gain (G_m) stage using a switched-*LC* N-path feedforward network (N=4 in this work) to enhance the OOB rejection (see Fig. 3). Unlike the switched-*C* N-path network [3], that is based on a set of left switches (SW_L), series capacitor C_S and a set of right switches (SW_R), here we added a series-connected *inductor* L_{SH1} (15nH) at the input-side with capacitor C_{SH1} (80pF MIM), resulting in a low-frequency notch that is up-converted to RF by the left N-path. Thus, the input-side OOB rejection around LO frequency (f_{LO}) can be improved when compared to the topology of [3] as shown in Fig. 2(a), for equal-valued capacitors. In addition, a cancellation notch is provided at the output due to the out-of-phase addition of the currents generated by the G_m stage and N-path network. Thanks to L_{SH1}, C_{SH1} and C_{SH2} (52pF MIM), the cancellation notch sits closer to f_{LO}. Furthermore, the up-conversion of C_{SH2} provides an output-side bandpass response for improved interference handling at larger offset frequencies.

The large-signal linearity of the LNA is determined by its load impedance and G_m. The load impedance is dominated by the up-converted OOB impedance $Z_{RF,o}$ from the switched-*LC* N-path network. G_m (88mS) does not depend on the input level for peak input swings up to 0.9V as long as $Z_{RF,o}$ is close to zero. The output DC level of the G_m stage is set by mirroring it from a downscaled G_m replica under a DC feedback loop. A highly accurate (5mV step) tunable bias voltage for both the body (V_{BP} and V_{BN}) and the gate (V_{GP} and V_{GN}) of the G_m enables optimization of the small-signal linearity. All bias can be programmed through a serial-parallel interface.

A. Switched-LC N-path: Input and Output Close-by Notch

By introducing a shunt inductor L_{SH1}, a low impedance is created at its resonance frequency with C_{SH1} and up-converted to the LNA's input due to the frequency-translational property of the N-path filtering technique. The input RF impedance $Z_{RF,i}\{\omega_{LO}+\Delta\omega\}$ is

$$Z_{RF,i}\{\omega_{LO}+\Delta\omega\} \approx R_{SWL} + \left(\frac{2}{\pi}\sin\left(\frac{\pi}{4}\right)\right)^2 \cdot Z_{BB,i}\{\Delta\omega\},$$

where R_{SWL} is the on-resistance of the N-path switch SW_L, and $Z_{BB,i}\{\Delta\omega\}$ is the equivalent input-side BB impedance. When R_{SWL} is small enough, $Z_{RF,i}\{\omega_{LO}+\Delta\omega\}$ is dominated by $Z_{BB,i}\{\Delta\omega\}$. Also, at the resonance frequency $Z_{BB,i}\{\Delta\omega\}$ is dominated by the low impedance created by L_{SH1} and C_{SH1}. When $\Delta\omega$ increases, C_S (52pF) and C_{SH2} affect $Z_{BB,i}\{\Delta\omega\}$ more. As shown in Fig. 4, thanks to the close-by notch created by L_{SH1} and C_{SH1}, the proposed topology achieves 3.9 and 1.8dB additional input rejection at the left-/right-side of f_{LO} compared to the switched-*C* N-path topology for equal capacitor sizes. In addition, the simulated in-band IM_3 improves 13.2dB when TX signal and jammer

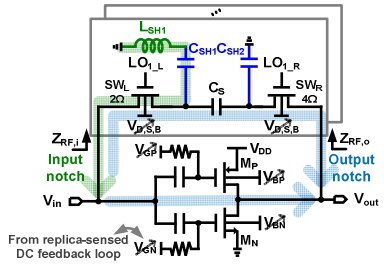

Fig. 3. Proposed switched-*LC* N-path LNA with Class-A/B G_m.

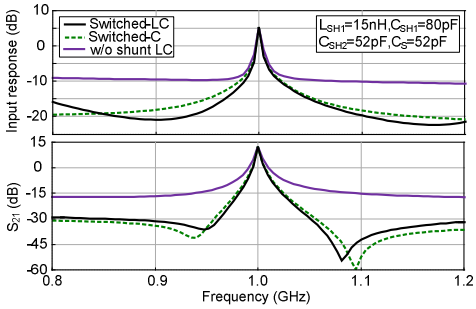

Fig. 4. Simulated frequency response for switched-*LC*, -C and regular N-path LNAs.

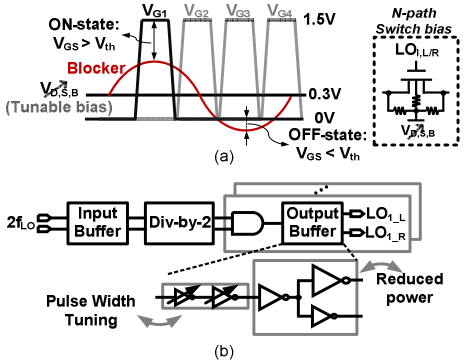

Fig. 5. (a) N-path optimum-biasing at large-signal operation and (b) 25%-duty-cycle LOGEN.

appears at left-side 40 and 80MHz offset. The notch position at the output depends on the size of the shunt capacitors C_{SH1} and C_{SH2}, and it will move toward f_{LO} when enlarging C_{SH1} and C_{SH2}. Thanks to the shunt inductor L_{SH1}, the notch offset is 30% and 18% reduced for the left-/right-side of f_{LO}, respectively.

The inductor adds an extra degree of freedom to the trade-off between power and rejection for N-path filters. The power consumption of this LNA is thus reduced compared to sub-100nm implementations with similar rejection [3], [4], even when using 0.18µm SOI CMOS, which has a much lower f_T.

To ensure the OOB rejection is not limited by the on-resistance of the N-path switches, R_{SWL}=2Ω (SW_L: 160/0.18µm) and R_{SWR}=4Ω (SW_R: 80/0.18µm) is selected. The SW_R size is reduced since it does not impact the input filtering response, deemed most critical to combat OOB

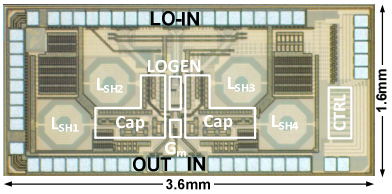

Fig. 6. Chip photograph of the LNA in 0.18µm SOI CMOS.

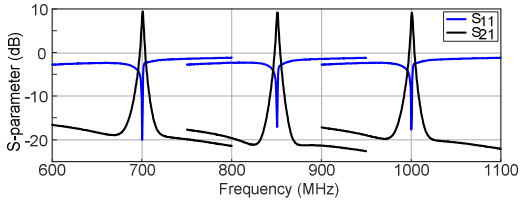

Fig. 7. Measured S-parameter at 0.7 to 1GHz f_{LO} (default mode).

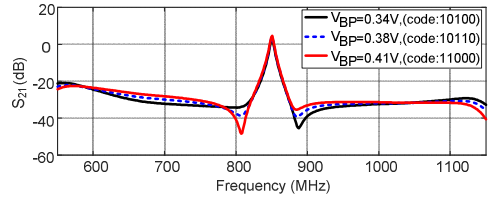

Fig. 8. Measured S_{21} in high-rejection mode with notch tuning.

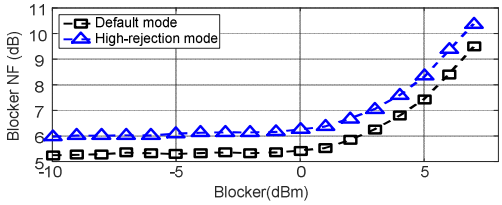

Fig. 9. Measured blocker NF.

interference. Simulation shows that 10.5mW of dynamic power is saved due to the smaller SW_R, at the expense of 4.5dB output rejection.

B. N-Path with Optimum-Biasing

The gate/drain/source bias ($V_{G,D,S}$) of the N-path switches should be considered for both ON and OFF periods. During the ON period, the voltage difference, V_G–V_S, must be maximized in order to achieve a low switch R_{ON}. In fact, the LO swing should be greater than the maximum swing of the interference by at least one threshold voltage V_{th} (Fig. 5(a)). During the OFF period, a negative voltage difference of V_G-V_S helps to prevent any undesired turn-on of the N-path switches when a large interference is present. Here, we make sure the minimum LO swing is below the interference swing by at least one V_{th} during the OFF period (Fig. 5(a)).

With an LO swing between 0 and 1.5V, the optimum N-path switch bias ($V_{D,S,B}$) is 0.3V, which leads to a simulated OOB-iB$_{1dB}$ of +13.2dBm. The OOB-iB$_{1dB}$ drops by 3.3dB for $V_{D,S,B}$=0V, which implies the OFF state cannot be handled well. Also, the OOB-iB$_{1dB}$ will degrade by 4.5dB if a fixed $V_{D,S,B}$=0.6V is set (i.e., the body terminal of the switch is connected with the drain/source). The linearity of the LNA is closely related with the LO swing. The simulated OOB-iB$_{1dB}$ could reach +19.2dBm when a 2V LO swing and $V_{D,S,B}$=0.7V was used. Unlike [3], that uses AC-coupling to aid the LO biasing, the overdrive voltage of the N-path switches is adjusted here by programming $V_{D,S}$. This approach avoids the parasitic capacitance of the AC-coupling capacitors from degrading the effective LO swing and the LOGEN's power efficiency.

C. Power-Optimized Low-Noise 25%-Duty-Cycle LOGEN

A low-noise div-by-2 LOGEN [5] is developed as shown in Fig. 5(b), where the divider does not contribute noise to LO output waveforms. The output buffer of LOGEN is designed with 4 inverter stages, where the first 2 stages are designed in a tunable fashion to allow for changing the pulse width of LO waveforms (±10% range), and the last 2 stages are designed with a fan-out of 2 and 0.6 in terms of equivalent capacitive load to both enable the drive of the large SOI N-path switches, and optimize the power consumption. The simulated phase noise is -165dBc/Hz with 57.2mW dynamic power at 1GHz.

III. Measurement Results

Fig. 6 shows the LNA photograph. It is fabricated in 0.18µm SOI CMOS and occupies an active area of 2.2mm^2. The LNA was measured RF$_{IN}$ to RF$_{OUT}$, with 2x off-chip L-C networks to aid input- and output impedance matching, using 50-Ω instrumentation without any RF buffers. Supplied at 1.5V, the power consumption ranges from 48.4mW (0.7GHz) to 62.5mW (1GHz), of which 5.3mW is consumed by G_m. The remainder is the LOGEN's dynamic power consumption.

In the default mode, Fig. 7 plots the measured S_{21} and S_{11}, where the passband gain ranges from 9.1 to 9.6dB, and the OOB rejection varies from -31.2 to -28.6dBc at 40MHz offset. In-band, S_{11}<-15dB is consistently measured at different bands when changing only the LO frequency (i.e. no further tuned matching is done). The passband has a -3-dB bandwidth of 3.6MHz, which could be enlarged by downsizing C_S (fixed in this design). The NF measures between 4.6 to 5.7dB from 0.7 to 1GHz.

In the high-rejection mode, the OOB rejection is enhanced by tuning the body bias voltage of the PMOS transistor in the G_m, and using a slightly overlapped LO waveform, as well as a lower $V_{D,S,B}$ bias voltage for the N-path switches (i.e., smaller R_{ON}). This mode offers a deeper cancellation notch at the cost of 4.2dB reduction of the passband gain. The notch can be tuned to be either at the left- and right-side of f_{LO}. Fig. 8 shows that ≥45dBc output rejection (left or right) at a 40MHz offset can be achieved.

As shown in Fig. 9, the measured blocker NF is 9.5dB (default mode) and 10.4dB (high-rejection mode) at a +7dBm CW blocker at 40MHz offset (from a 865MHz LO frequency). For default mode, it is estimated from simulation that 3.6dB of the blocker NF is due to reciprocal mixing with the LOGEN's phase noise, and another 0.7dB is due to the gain compression of G_m.

Fig. 10 shows the measured OOB-IIP$_3$ in which the two tones are located at 785 and 825MHz and the IM3 tone is located (in-band) at 865MHz. The OOB-IIP$_3$ is +26.2 and +32.2dBm for the default and high-rejection modes, respectively. Fig. 11 presents the input-referred OOB-blocker-caused in-band gain compression, OOB-iB$_{1dB}$, versus the blocker offset frequency. OOB-iB$_{1dB}$ is measured as +8dBm at 40MHz offset and up to +9.1dBm at larger offsets.

Table I lists the performance summary and compares this work with the state-of-the-art. This work enhances the OOB RF-rejection at smaller frequency offset and achieves better blocker NF, while also achieving low power consumption, at comparable gain, NF and OOB linearity.

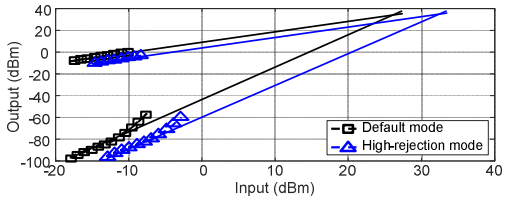

Fig. 10. Measured OOB-IIP$_3$ at 40MHz offset.

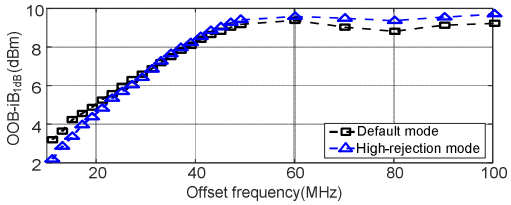

Fig. 11. Measured OOB-iB$_{1dB}$ versus blocker offset frequency.

TABLE I. COMPARISON WITH STATE-OF-THE-ART

	This work		*TMTT'16* [3]	*RFIC'15* [4]	*JSSC'12* [6]
	Default	*High-rejection*			
Gain (dB)	9.1-9.6	3.8-4.6	5.4-11.5	-4.7~-6.2	72
Notch offset (MHz)	40	40	250*	60*	N/A
Output Rejection @ Notch (dBc)	-31.2	-50.3	-50*	-22*	N/A
OOB-iB$_{1dB}$ (dBm)	+8 @40MHz	+8 @40MHz	+11 @50MHz	+9 @40MHz	+3* @50MHz
OOB-IIP$_3$(dBm)	+26.2 @40MHz	+32.3 @40MHz	+36 @50MHz	+17.5 @80MHz	+19* @40MHz
NF (dB)	4.6-5.7	5.5-6.4	3.6-4.9	8.6	1.9
Blocker NF (dB) @ +4dBm P_B	6.8	7.4	14*	N/R	13*
Power (mW)	48.4-62.5	42-57.3	81-209	75	35.1-78
What?	LNA		LNA	Filter	Full RX
Frequency (GHz)	0.7-1		0.4-6	0.6-0.85	0.08-2.7
LO Supply (V)	1.5		2	1.2	1.3
Analog Supp. (V)	1.5		N/R	1.2	1.3
Active area(mm^2)	2.2		0.28	1.2	1.2
Techno. (CMOS)	0.18µm SOI		32nm SOI	65nm	40nm

N/R: Not Reported, N/A: Not Applicable, *Estimated from figures

IV. CONCLUSIONS

This paper introduced a gain-boosted, switched-*LC* N-path LNA that achieves at a >40MHz offset to realize a self-interference resilience for the FDD-LTE low bands covering 0.7 to 1GHz. Furthermore, a power-optimized low-noise LOGEN is employed to reduce reciprocal mixing impact on NF. The LNA is implemented in 0.18µm SOI CMOS and achieves >30dB RF rejection at ≥40MHz offset and 6.8dB blocker NF at +4dBm blocker power. It has a +26.2dBm OOB-IIP3 and an OOB-iB$_{1dB}$ of +8dBm, all at a reasonable power consumption of 48.4mW (0.7GHz) to 62.5mW (1GHz). The LNA also offers a tunable cancellation notch measuring an output rejection of >50dBc when reconfigured to the high-rejection mode.

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