A 0.4V 4.8µW 16MHz CMOS Crystal Oscillator Achieving 74-Fold Startup-Time Reduction Using Momentary Detuning

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***Abstract*—For ultra-low-power radios, the long startup time of the crystal oscillator dominates their on-off latency and limits their power efficiency. This paper describes the design of a 65nm CMOS 16MHz crystal oscillator, featuring a momentary detuning scheme to accelerate the startup transient. Specifically, during the startup phase, the bias current (266µA) and loading capacitors (8.5pF each) are enlarged concurrently such that the equivalent negative resistance of the oscillation loop can be momentarily enhanced, resulting in 74-fold reduction of the startup time (37ms → 0.5ms), while consuming just 53.2nJ at 0.4V. Also, a time-based controller automatically drives the oscillator into the steady state, which entails a smaller bias current (12µA) to sustain the oscillation, and smaller loading capacitors (5pF) to recover the proper oscillating frequency. The simulated phase noise exhibits -128.2dBc/Hz at 1kHz offset, resulting in a FoM of 265.5dBc/Hz.**

***Keywords*—CMOS; crystal oscillator; fast startup; low-voltage; low-power; ultra-low-power.**

I. Introduction

Benefitting from the excellent quality factor of the quartz crystal in the kHz to MHz range, a Crystal Oscillator (XO) offers a much more stable and precise reference clock signal than its RC and ring counterparts, dominating their utility in a wide variety of applications such as wireless transceivers. Albeit the performance and characteristics of the XO have been studied for years [1], only recent efforts have started to focus on its historic problem of long startup time (t_{start}). A long t_{start} hinders the effectiveness of the XO in ultra-low-power wireless radios. For Bluetooth-Low-Energy that operates in a duty-cycle mode [2], the XO has to be powered down periodically to save the battery. Thus, a short t_{start} is essential to reduce the on-off latency in launching a connection and enhance the power efficiency [3].

To shorten t_{start}, for instance, [4] proposed a digitally-calibrated frequency injection technique. It employs a ring oscillator to generate an injection signal to the crystal. Regrettably, as the ring oscillator is sensitive to PVT variation, generating an output frequency close enough to the resonant frequency of the crystal is non-trivial without calibration, complicating the design of the XO.

This paper reports a fast-startup XO employing a momentary detuning technique (Fig. 1), avoiding any auxiliary oscillator with precise tuning and buffer that otherwise degrade the startup energy efficiency of the XO. In fact, by properly boosting the transconductance and capacitive load of the XO during the startup transient, the negative resistance can be risen to speed up its oscillation. Also, a low supply voltage is applied to prepare this work for energy-harvesting applications.

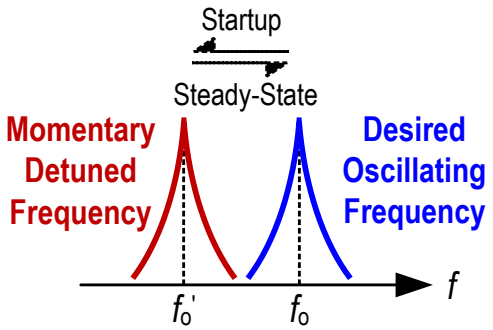

Fig. 1 Illustration of the crystal detuning scheme in the frequency domain.

II. Proposed Fast Startup Crystal Oscillator

A. Analysis on the negative resistance of the amplifier

We use the typical Pierce XO [Fig. 2(a)] to show how the negative resistance of the amplifier affects the startup time of the XO. The crystal with a designated oscillating frequency (f_o) is connected in parallel with the core amplifier (g_m) and feedback resistor (R_F) that serves for self-biasing. Typically, each crystal is specified with an adequate load capacitance (C_L) to operate at the appointed f_o. The core amplifier can be a common-source amplifier with an active load, which controls the bias current of the core amplifier. A crystal can be modeled by an RLC network for electrical characterization [Fig. 2(b)]. L_m and C_m represent the motional arm inductance and capacitance of the crystal; they together determine the series resonant frequency. R_m is the real physical energy loss of the crystal during vibration. The stray capacitance of the crystal package is denoted as C_s.

To activate and sustain the XO oscillation, the amplifier has to compensate the resistive loss of the crystal. Fig. 2(c) shows the schematics to derive the input impedance Z_c of the amplifier together with the stray capacitance seen from the crystal. The equivalent circuit to derive Z_c is shown in Fig. 2(d), where r_o is the output impedance, g_m is the transconductance, and C_{GD} is the parasitic capacitance between the gate and drain of the core amplifier, respectively. Cs can be added up with C_{GD} and denoted Cs'. Assuming R_F and r_o are much larger than the impedance of Cs' and C_L, at the oscillation frequency (i.e., $j\omega R_F C_s' \gg 1$ and $j\omega 2 r_o C_L \gg 1$), the real part of Z_c can be derived as [1]:

$$Re(Z_c) \equiv -R_N = -\frac{4g_m {C_L}^2}{(g_m C_s')^2 + 16\omega^2({C_L}^2 + C_s' C_L)^2} \quad (1)$$

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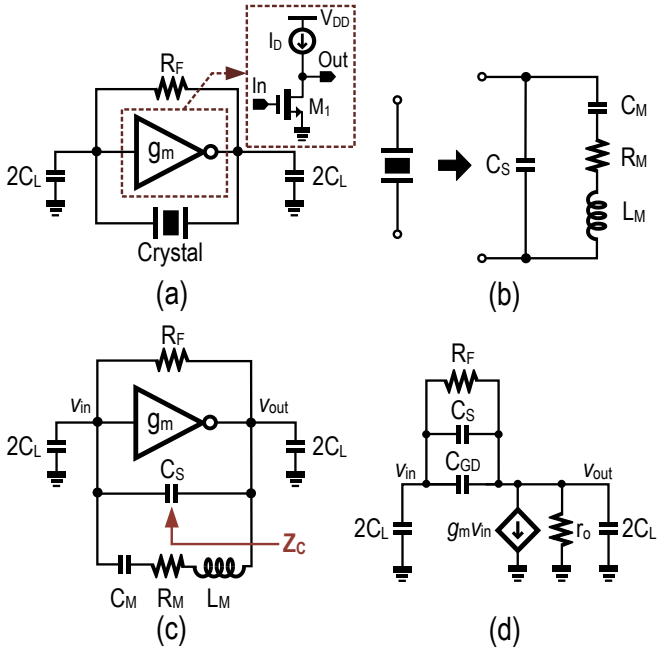

Fig. 2 (a) Schematic of the basic Pierce oscillator; (b) Electrical model of the quartz crystal; (c) Schematic of the Pierce oscillator for deriving Z_C; (d) The equivalent circuit for deriving Z_c.

This R_N not only determines if the XO will oscillate, but also if it affects the t_{start} of the oscillator, which is proportional to the time constant τ and can be expressed as:

$$\tau = \frac{L_M}{R_N - R_M} \tag{2}$$

It is obvious from (2) that R_N should be increased to suppress t_{start} of the XO. A straightforward way to boost R_N is to increase the g_m of the core amplifier [5]. Yet, R_N is not a monotonic function of g_m, as (1) illustrates. Instead, it will start to decrease from the optimal value after a certain g_m, which can be derived by equating the derivative of (1) to zero:

$$g_{m,opt} = 4\omega C_L\left(1 + \frac{C_L}{C_s'}\right) \tag{3}$$

with the corresponding R_N at $g_{m,opt}$ as:

$$R_{N,opt,gm} = \frac{C_L}{2\omega C_s'(C_s' + C_L)} \tag{4}$$

When the actual g_m exceeds $g_{m,opt}$ at the designated C_L, R_N will drop, degrading the power efficiency of the XO. Instead, as shown in (4), $R_{N,opt,gm}$ can be enlarged by raising C_L. Inspired by this, the limit of R_N can be averted by altering both g_m and C_L of the XO. To exemplify this, Fig. 3(a) reveals a contour plot of R_N with respect to g_m and C_L. For instance, with a C_L of 5pF, the peak R_N of the XO is ~400Ω with a g_m of 4.2mS [Fig. 3(b)]. The R_N does not increase even a higher g_m is set. Yet, if C_L increases together with g_m, the $R_{N,opt,gm}$ can be raised further as given in (4). In fact, the maximum achievable $R_{N,opt,gm}$ is confined by several factors. Firstly, as depicted in (4), $R_{N,opt,gm}$ is bound by $1/2\omega C_s'$ (for $C_L \gg C_s'$). For instance, with C_s'=5pF at an oscillating frequency of 16MHz, the theoretical maximum of R_N is 995Ω. Secondly, when the transistor is upsized to generate a

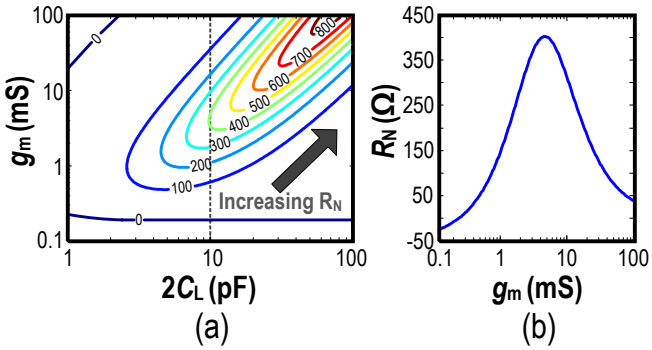

Fig. 3 (a) The contour plot of R_N against C_L and g_m; (b) The R_N versus g_m at C_L=5pF. For both figures, f_o=16MHz, R_F=2MΩ, r_o=5kΩ, Cs'=5pF.

larger g_m (using more I_D), its parasitic capacitances and limited output impedance in deep submicron CMOS process will deteriorate R_N. Particularly for C_{GD} that will increase C_s' and thus degrades the maximum R_N. Further, as r_o is inversely proportional to I_D, raising I_D will degenerate R_N when r_o is non-negligible if compared to the load capacitance.

B. Momentarily detuning technique for fast XO startup

As manifested above, detuning the crystal by increasing both g_m and C_L simultaneously can boost R_N, resulting in a shorter t_{start}. Yet, this detuning will pull away the actual resonant frequency of the XO from f_o to f_o', the detuned oscillating frequency. Such a deviated f_o' can affect the correlated blocks in the transceiver. Further, raising g_m of the amplifier incurs in higher active power consumption unwelcome for ultra-low-power applications.

To this end, we propose a momentarily detuning technique for the XO. It leverages the compromise between a fast t_{start} by boosting the g_m and C_L (thus R_N) during the starting transient, and a low power consumption at the steady state by returning the g_m and C_L to their nominal values, such that R_N is just enough to sustain the oscillation of the XO. A master control signal EN_{DT} synchronously controls the bias current I_D (thus the g_m) and C_L in the starting phase, once the XO is triggered (i.e. upon turning on V_{DD}) to increase the R_N of the XO [Fig. 4(a)]. Changing C_L is feasible as the frequency accuracy is irrelevant in this startup period. When the amplitude of oscillation reaches the desired value, the EN_{DT} signal will be disabled [Fig. 4(b)]. C_L is then returned back to its designated value, and I_D is lowered. In this way, the XO can accommodate a fast t_{start} during the startup, and low active power consumption in the steady state.

In the design, to automatically manage the duration of EN_{DT}, we add a comparator (ADC) and a counter as a time-based controller. The comparator formed by inverters digitizes the oscillation signal after sufficient oscillation occurs. Then, the digitized signal is delivered to the counter, which counts the number of pulses (N) of the digitized signal. Once N reaches the allocated value, EN_{DT} will be disabled, letting the XO to enter into the steady-state. This self-contained time-based detection is programmable, and less prone to amplitude variation, culminating in a delicate control on the pulse width. Further, when compared with the amplitude-based detection, this time-based detection features lower power consumption as it does not entail any analog modules consuming considerable static power.

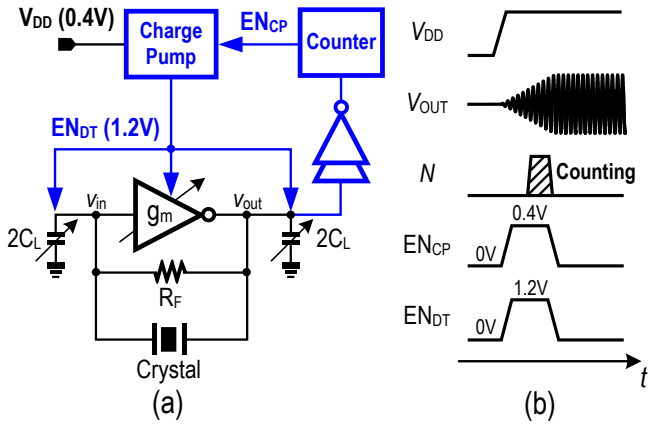

Fig. 4 (a) Schematic of the proposed XO with the control electronics for detuning (highlighted in blue); (b) Timing diagram of the operation of the proposed XO.

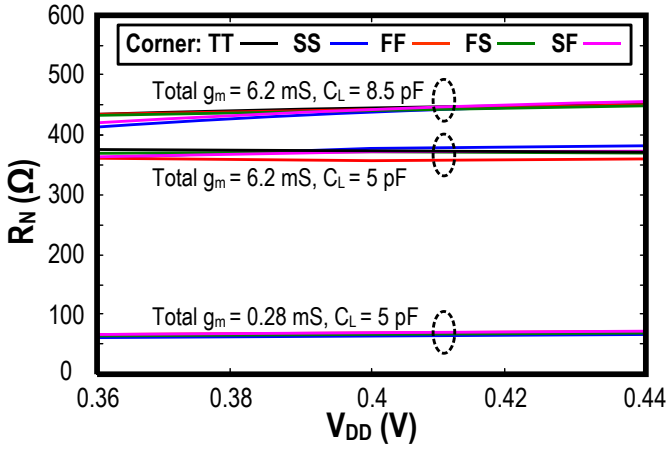

Fig. 5 Simulated R_N of the XO at 16MHz with different set of g_m and C_L versus process variation (5 process corners) and supply voltage (±10%) at 27°C.

III. Simulation Results

The XO is designed and simulated in a typical 65nm CMOS process. All circuit components, except the crystal, are implemented with on-chip elements. The crystal frequency is chosen at 16MHz, which is common for ultra-low-power radios [6]. To prepare the XO for solar energy harvesting (e.g., photovoltaic harvester [7]), we select a low supply voltage of 0.4V. The voltage level of the EN_{DT} signal is boosted to 1.2V by an internal two-stage charge pump to ease the mode switching. As those switches do not consume static power and are only enabled during the startup phase, the effect on the overall XO power efficiency is negligible. The charge pump consumes 0.45µW and the ripple on the output is ~2.7mV, with a starting time of 1.5µs. The counter and the comparator consume <1µW dynamic power and are also disabled in the steady state.

Fig. 5 depicts the simulated R_N of the XO. In the steady state, we design R_N of the XO at a value greater than R_m (60Ω) of the crystal, with g_m of 0.28mS (I_D=12µA) and C_L of 5pF, which matched the specified load capacitance of the crystal. Yet, the corresponding t_{start} of the oscillator is long with this R_N. As verified from the transient simulations, t_{start} with such setup is ~37ms [Fig. 6(a)], which is much slower when compared with other XOs reported in the literature. If the amplifier g_m increases

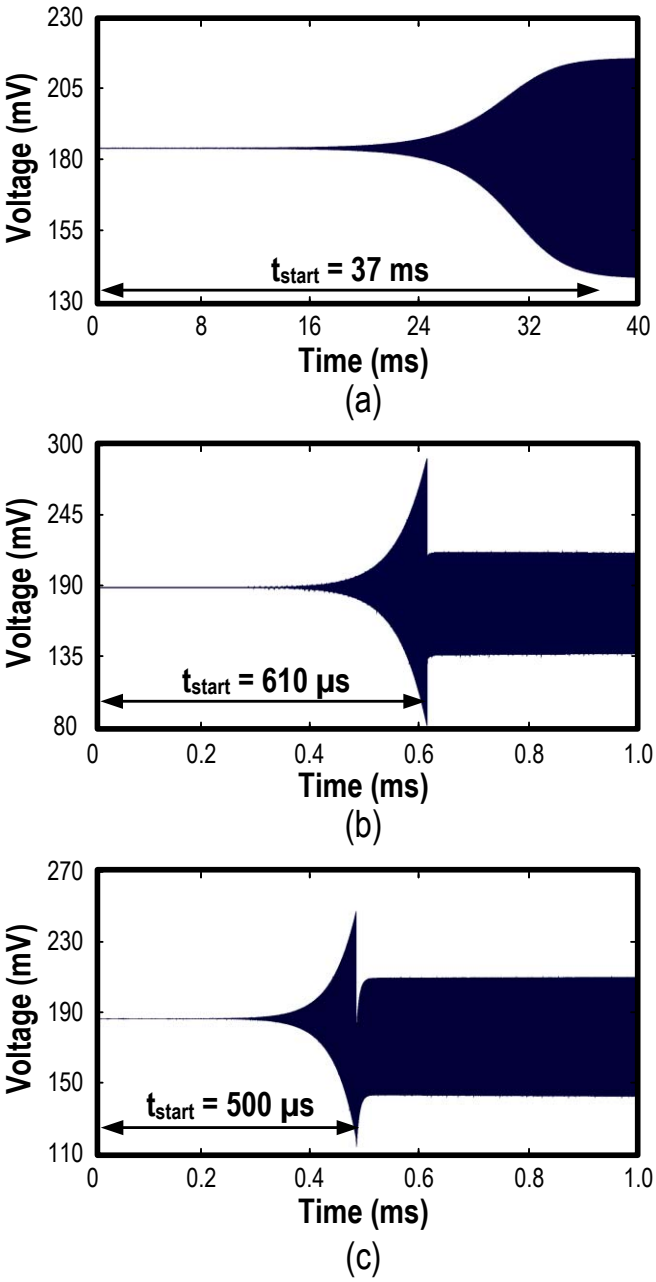

Fig. 6 Startup time of the XO. (a) Without boosting g_m and C_L; (b) g_m = 6.2mS and C_L = 5pF in the startup phase; (c) g_m =6.2mS and C_L = 8.5pF in the startup phase.

to 6.2mS (I_D=266µA), R_N can be resized to ~371Ω. After the crystal has gained enough energy, the EN_{DT} signal is cut off and g_m will be switched back to the steady-state mode (0.28mS). Correspondingly, t_{start} of the XO will be soothed to 0.61ms [Fig. 6(b)]. Finally, if the C_L is also increased to 8.5pF together with g_m, R_N of the XO will be further increased to ~445Ω, rendering a better power efficiency than the case without increasing C_L as the power consumption is identical. t_{start} in this case will be further improved to 0.5ms [Fig. 6(c)], which reveals a 74-fold reduction from the case without boosting g_m and C_L and also 22% less than the case that only increases g_m. This corresponds to a startup energy (i.e., $V_{DD} \times I_D \times t_{start}$) of 53.2nJ in line with the state-of-the-art.

TABLE I. PERFORMANCE COMPARISON WITH PREVIOUSLY REPORTED XOS.

	TCAS' 12 [4]	JSSC '12 [8]	VLSI '14 [5]	ISSCC '16 [9]	ISSCC '16 [3]		This Work *	
CMOS Process (nm)	180	65	180	65	65		65	
Supply Voltage (V)	1.8	1.8	1.5	3.3	1.68		**0.4**	
Frequency (MHz)	32	26	39	39.25	24		16	
Startup Time (ms)	0.05	3.2	0.16	3.9	0.064	0.435	**0.5**	
Startup Energy (nJ)	N/A	6976	434	74.1	N/A	N/A	**53.2**	
Steady-State Power (μW)	N/A	2180	181	19	390	690	**4.8**	**14.4**
Phase Noise @1kHz Offset (dBc/Hz)	N/A	-136	N/A	-139	N/A	N/A	**-128.2**	**-139.8**
FoM # @1kHz Offset (dBc/Hz)	N/A	251	N/A	278	N/A	N/A	**265.5**	**272.3**
Fast Startup Technique	Digitally Calibrated Injection	None	Chirp Injection & R_N Booster	None	Dithered Frequency Injection		**Momentary Detuning**	
Auxiliary Oscillator for Startup Excitation	Yes	None	Yes	None	Yes		**None**	

*Simulation Results # FoM = (Oscillation frequency)²/[Power x (Offset frequency)² x Phase noise]

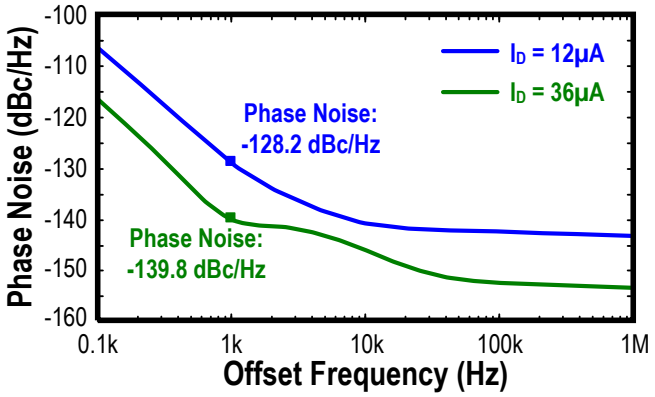

Fig. 7 Simulated PN of the XO versus offset frequency with varying bias condition.

Fig. 7 shows the simulated phase noise (PN) of the XO. With a bias current of 12μA, the PN at 1kHz offset from the oscillating frequency is -128.2dBc/Hz, and the corresponding FoM is 265.5dBc/Hz. For applications that entail a better PN, I_D can be enlarged to magnify the oscillation amplitude and suppress the thermal noise of the amplifier. For instance, when I_D is tripled, both PN and FoM will be improved to -139.8dBc/Hz and 272.3dBc/Hz at 1kHz offset, respectively. The noise floor is also improved from -143 to -153dBc/Hz.

Table I summarizes the performance and compares this XO with the others. This work exploits only switchable bias and load capacitors to achieve a faster startup, while avoiding the raise of power consumption in steady state. If compared to other XOs with different fast startup techniques, herein the proposed technique eliminates auxiliary ring oscillators and buffers to inject a precise signal to the crystal, which otherwise increases system's complexity and power consumption.

IV. CONCLUSIONS

This work has revealed a power-efficient detuning scheme to improve the startup time of XO, using only switchable bias and load capacitors. To shorten the startup time, R_N of the core amplifier is enlarged by temporarily elevating g_m and C_L. After delivering adequate energy to the crystal for oscillation, the time-based controller reverts automatically g_m and C_L to their typical values to save power and attain proper oscillation frequency. By exploiting the proposed detuning scheme, the XO achieved a 0.5ms startup time and a 53.2nJ startup energy in simulations, without resorting to any auxiliary oscillators for frequency injection. With 4.8μW of power at a 0.4V supply, the simulated PN of the XO is -128.2dBc/Hz at a 1kHz offset, which is adequate for short-range communication. This renders the proposed work as a promising XO for ultra-low-power radios.

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