A Wide Range High Efficiency Fully Integrated Switched-Capacitor DC-DC Converter with Fixed Output Spectrum Modulation

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Abstract

This paper presents a wide range high efficiency fully integrated switched-capacitor DC-DC converter with fixed output spectrum targeting for noise-sensitive Internet-of-Things (IoT) applications. In order to alleviate the unpredictable output spectrum and the reduced energy efficiency of the conventional pulse-frequency modulation (PFM) and pulse-width modulation (PWM) schemes, fixed output spectrum (FOS) modulation is proposed to ensure easy noise filtering while achieving wide range high efficiency operation. A 2-phase 3-level gate driver is also proposed to minimize the reversion loss and enhance conduction. Simulation result in a standard 0.18-µm CMOS process shows that up to 88% high energy efficiency can be achieved with a loading range from 75µA to 3mA using a total flying capacitance of 0.96nF.

Key words: switched-capacitor DC-DC converter, fixed output spectrum modulation, EMI

Introduction

Switched-capacitor DC-DC converter (SC-DCDC) is widely employed in portable devices for high efficiency and low Electro-Magnetic Interference (EMI) voltage conversion [1]. Depending on whether the devices operate in heavy load or light load mode, the loading level varies drastically [2]. Thus, to prolong the system lifetime, high energy efficiency over a wide loading range is required. Moreover, noise reduction is also critical for powering sensitive circuits such as the wireless communication module [2].

Pulse-frequency modulation (PFM) is a well-known technique to improve light-load efficiency as it adjusts switching frequency according to the load current. However, the varying output spectrum prohibits efficient noise filtering that may degrade the performance of sensitive devices. Compared with PFM, fixed output spectrum (FOS) regulation is generally preferred due to its predictability in the output spectrum. Previous fixed output spectrum regulation methods include: a) Pulse-width modulation (PWM) control, which controls the amount of transfer charge by adjusting the duty cycle. b) Charging current control (CCC) [3, 4], which varies current source or gate driver numbers to control the charge current to achieve output power regulation. However, their loading range is relatively narrow. In light load, they require high operating frequency that introduces large switching loss, hence deceases the conversion efficiency considerably.

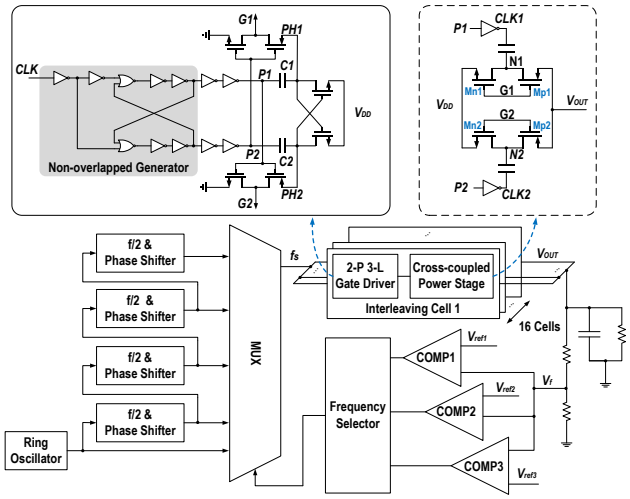

Fig. 1 The proposed SC-DCDC block diagram.

One solution to the reversion current loss in the conventional cross-coupled SC-DCDC is to use two pairs of non-overlapped signals [5]. This can be achieved via level shifter and gate control strategy. However, the timing mismatch of the 4-phase clock may introduce further reversion loss [6].

To achieve high energy efficiency over a wide loading range, a FOS scheme is proposed. It retains the advantages of other FOS such as PWM and CCC, yet the 2-phase 3-level (2-P 3-L) gate driver only uses one pair of gate control signal to prevent reversion current and provides a large driving current.

System Architecture

A. Architecture

Fig.1 shows the block diagram of the proposed SC-DCDC. The ring oscillator is to provide a fundamental clock for the system. 4 frequency dividers and phase shifters are used to generate extra clock signals with different frequencies. One of these clocks are selected and fed into the interleaving cells to generate V_{OUT}. Depending on the loading condition, the frequency selector may change the switching frequency to optimize its performance.

B. Conversion Efficiency Enhancement

The SC-DCDC optimizes its light-load conversion efficiency by stepwise adjusting its switching frequency f_s. Since the total

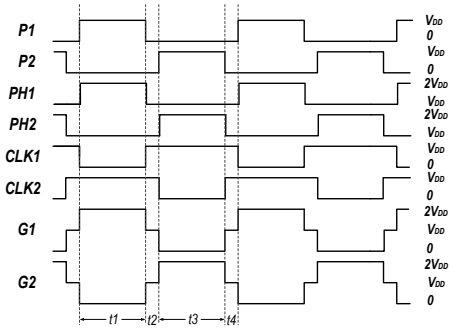

Fig. 2 The timing of proposed SC-DCDC.

loss is dominated by the switching loss at light load, which is proportional to f_s, reducing f_s would enhance the energy efficiency substantially.

A 2-P 3-L gate driver is also proposed to alleviate the reversion loss and enhance conduction in order to improve the efficiency. Fig.2 shows the corresponding timing diagram. A 2-phase clock (*G1*, *G2*) is generated via the 2-P 3-L gate driver. These clocks are then used to control the cross-coupled power stage for the SC-DCDC's operation. In the steady state, nodes *N1* and *N2* swing between V_{DD} and $2V_{DD}$. To turn on the NMOS pair, the gate driver signal should be higher than V_{DD}. *G1* and *G2* are a pair of non-overlapped high clock to prevent the reversion current flows through the NMOS pair. Although the PMOS pair Mp1, Mp2 are turned on simultaneously at t2 and t3, nodes *N1* and *N2* are at the same potential thus no reversion current is introduced. Furthermore, *G1* and *G2* also use lower voltage 0 to turn on Mp1, Mp2 reducing their on-resistance and enhancing the current driving capability.

C. Fixed Output Spectrum Modulation

When V_{OUT} is changed due to variation in the load, V_f will be changed accordingly. As a result, the frequency selector selects another frequency f_s to ensure V_{OUT} recovers to 1.8V quickly. When f_s is decreased by a factor N, its output spectrum also decreases N times. However, using M interleaving phase could increase the output spectrum M times. Based on this observation, we match M with N to obtain a fixed output spectrum. In this design, we have 5 operating frequencies by tuning $N = 2^i$, where $0 \le i \le 4$.

Simulation Results

The proposed SC-DCDC is implemented in standard 0.18-µm CMOS technology. With *CLK* = 15 MHz and a total flying capacitance of 0.96nF (*C1* and *C2* in Fig. 1). Fig. 3 shows the simulated conversion efficiency with and without 2-P 3-L gate driver, as well as the comparison with the conventional PWM and CCC schemes. The proposed SC-DCDC boosts 1V to 1.8V over a loading range between 75µA and 3mA with peak conversion efficiency of 88%. As mentioned, the output spectrum regulated by PWM or CCC has low light-load efficiency caused by large switching loss. By frequency control using the interlacing cells, the proposed SC-DCDC achieves the conversion efficiency improvement over 30% in the lightest load. Additionally, 2-P 3-L gate driver contributes around 5% efficiency improvement. Fig.4 shows the transient response. The recovery time is 0.5µs for undershoot and 8.5µs for overshoot. Table I summaries the simulation results and performance comparisons.

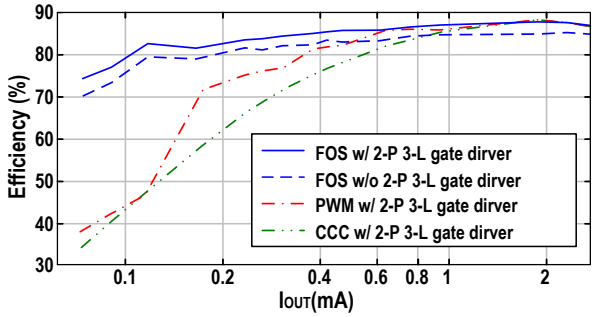

Fig. 3 SC-DCDC conversion efficiency with and without 2-P 3-L gate driver with different fixed output frequency regulation.

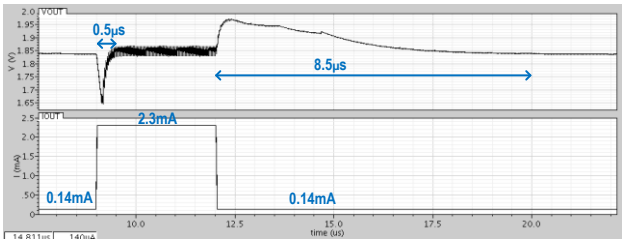

Fig. 4 Transient response.

TABLE I
PERFOEMANCE COMPARISON

	VLSI 2009 [1]	TCAS-I 2013 [3]	TCAS-II 2012 [7]	This work
Technology	180nm	350nm	65nm	180nm
Modulation Scheme	PFM	PWM	VRF-PDM	FOS
V_{in} (V)	1	1.8-5	1	1
V_{out} (V)	1.8	3.3	0.5	1.8
I_L (mA)	0.08 – 1.5	1 – 30	0.05 – 10	0.075 – 3
C_{flying} (nF)	0.4	2000	4.7	0.96
f_{OUT} (MHz)	<20	0.1	10	15
Efficiency	71%-82%	50%-82%	73%-86%	74%-88%

Conclusion

A high efficiency SC-DCDC with fixed output spectrum is presented. The proposed design converts a 1V supply to 1.8V with a fixed output spectrum. It has a wide loading range from 75µA to 3mA with conversion efficiency between 74% and 88%.

Acknowledgement

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