Ultra-low Power QRS Detection using Adaptive Thresholding based on Forward Search Interval Technique

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Abstract

We present an energy efficient QRS detector for real-time ECG signal processing implemented in ASIC. An adaptive thresholding scheme based on forward search interval (FSI) algorithm together with simple preprocessing is proposed to accurately detect QRS peaks. The Verilog HDL codes with improved hardware utilization efficiency are validated using FPGA, achieving 99.59% sensitivity (Se) and 99.63% positive prediction (Pr) using the MIT-BIH Arrhythmia database. A chip prototype is also implemented in a standard 0.18-µm CMOS process. Synthesized with a customized sub-threshold digital library for minimum energy operation, the proposed QRS detector occupies an active area of 0.13 mm^2 and consumes merely 93nW.

Introduction

Wireless ECG device for QRS complex analysis is one of the best candidates for long-term cardiac condition monitoring [1], with the requirements of high detection accuracy and reduced computational resources to improve the system lifetime. Many QRS detection algorithms suitable for application specific integrated circuit (ASIC) implementation have been published in recent years. Frequency domain processing algorithms focused on improving the detection accuracy using complex signal transformations and derivatives as well as digital filtering to maximize the signal-to-noise ratio (e.g. the popular wavelet transform (WT) algorithm [1]). However, the use of a set of analyzing functions is computationally expensive due to extensive multiplications. For ultra-low power ASIC implementations, the time domain level-crossing algorithm [2] is a promising candidate due to its reduced design complexity and power consumption at the expense of reduced detection accuracy. To solve this problem, hybrid algorithm [3] has been presented and high detection accuracy (even comparable to the WT algorithm in [1]) is demonstrated. Yet, there still have room to further decrease the power consumption while maintaining the detection accuracy. This work proposes an adaptive thresholding scheme based on forward search interval (FSI) algorithm with simple preprocessing to achieve high accuracy and nW power consumption.

Proposed Algorithm

The proposed system is illustrated in Fig.1. The pre-processing stage includes moving average, differential, and absolute operation which aims to locate the QRS complex and identify its peaks. The pre-processed ECG signal contains the real QRS complex peak. We detect the rising edge of R-peak in a QRS complex and denote the value of the detected sample as QRS_{pre}. This algorithm uses FSI with an adaptive threshold to detect QRS complex peak. The forward search starts from the current peak to the next peak of the pre-processed output. We set the FSI to be 200ms according to the refractory period. The elimination of storing the pre-processed ECG samples in memory makes the ASIC implementation more power and area efficient.

We find the peak value (max_{FSI}) of the filtered ECG signal (AS) in each FSI. No detection is allowed for the first FSI after an R-peak is detected, and a new threshold (TH) is calculated with TH= max_{FSI}. The value of new TH could be quite high if premature ventricular contraction or artifact appeared. For that reason, it is limited to TH=1.5QRS_{pre} if the $max_{FSI} \geq 2.75QRS_{pre}$. TH will reach 93.75% of its previous value for the coming FSI, this number is derived based on the TH will be decreased to 70 % of its refreshed value at 1200ms. But if there is a high amplitude noise peak which has a maxim value greater than 2.75QRS_{pre}, TH will rise to 1.5 QRS_{pre}. In this way, the adaptive threshold automatically adjusted with the trend of ECG waveform.

We initially select the sample as an unconfirmed R-peak if its amplitude exceeds the adaptive threshold. To identify the unconfirmed R-peak, a buffer storing the last 4 RR intervals is used. For a normal physiology, the QRS complex peak to T-wave end duration is about 360ms and the RR interval duration of 0.6 to 1.2s [3]. Considering physiological characteristics and the individual situation, we choose an empirical parameter of 36%. If the time interval between unconfirmed R-peak to previous QRS peak R_{temp} is less than 36% of the mean value of RR interval buffer R_m, the unconfirmed R-peak is identified as a noise peak. Otherwise, it is confirmed as a valid QRS complex peak while refreshing QRS_{pre} and the RR buffer. The RR interval analysis reduces the false detection by using the QT duration with reference to the previous complex. Fig. 2 shows the simulated QRS detection result based on Tape#107 in the MIT-BIH Arrhythmia database.

Performance Evaluation

Two databases are utilized to evaluate the performance of the proposed FSI-based adaptive thresholding algorithm in MATLAB. For the MIT-BIH database, 99.56% sensitivity (Se) and 99.67% positive prediction (Pr) achieved where excluded episodes of ventricular flutter in record 207. For the QT database, the Se and Pr are 99.74%, 99.51% respectively. This approach achieves good accuracy on both databases due to the optimal threshold taking the trend of ECG waveform into consideration.

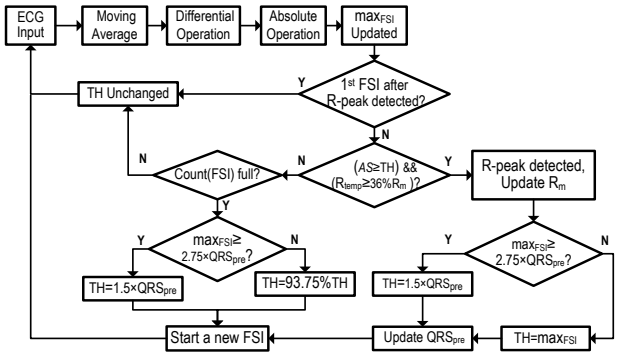

Fig.1 Architecture of the proposed system.

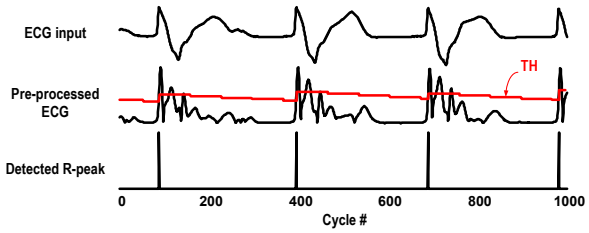

Fig.2. Simulation result of QRS detection @ Tape #107.

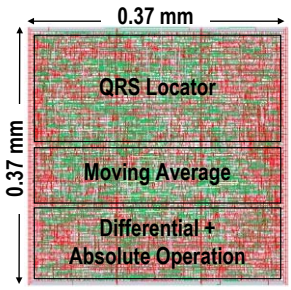

Fig.3. Chip Layout of the proposed ECG processor.

The proposed algorithm is first verified using MATLAB. The RTL implementation in Verilog HDL is verified using the Xilinx Spartan-6 FPGA platform for efficient ASIC design flow. The detection results on the MIT-BIH arrhythmia database show that the FPGA implementation achieves 99.59% Se and 99.63% Pr. The result has a slightly difference between software and hardware platform due to the limited bit-width. The pre-processing stage only performs the linear transformation of the ECG signals involving only addition and shifting operations. The proposed system only occupies 1000 logic elements, which is a 50% hardware resource reduction when compared with [4].

The ASIC implementation using a standard 0.18-µm CMOS process requires a total gate count of 3395. The layout of the chip is shown in Fig. 3, with a chip core area of 0.13mm^2. A customized 0.45V sub-threshold standard cell library [5] is used for reducing the system power consumption. A comparison with prior arts is given in Table I. All the verification results are obtained using the MIT-BIH arrhythmia database. It can be observed that the 4-scale WT algorithm [1] attains the highest accuracy, but with significant area/power overhead. The Harr WT [5] with reduced computational overhead consumes with good accuracy, but still consumes relatively high power. Even though the hybrid algorithm [3] has comparable accuracy when compared to WT [1], the power consumption is still high. The level-crossing algorithm [2] achieves good area/power performance at the cost of reduced accuracy, which is not acceptable for QRS detection systems. By balancing between complexity and detection performance, this work achieves comparable accuracy to [6] with significant area/power reduction.

TABLE I PERFORMANCE COMPARISON

Algorithm	Hybrid [3]	WT[1]	Level-cross[2]	Harr WT [6]	This work
Tech(µm)	0.13	0.18	0.13	0.18	0.18
Vdd (V)	0.6	1.1	0.3	1	0.45
Freq.(kHz)	1	32	1	N/A	10
Power(µW)	0.764	9	0.034	0.41	0.093*
Se%	99.85*	99.8	97.76*	99.6	99.59
Pr%	99.93*	99.86	98.59*	99.77	99.63
Area(mm^2)	0.22	1.2	0.1	0.484	0.13

* Simulation results only.

Conclusion

A high efficiency high accuracy real-time QRS complex detector is proposed. The MATLAB simulation results and FPGA measurement results show favorable performance when compared with prior arts. The proposed ECG signal processing system is also implemented in a standard 0.18-um CMOS process, achieving > 99.5% Pr and Se with merely 93 nW power consumption. The high accuracy, low power consumption, and small silicon area make this work especially suitable for long-term wireless health monitoring applications.

Acknowledgment

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