RESEARCH ABSTRACTS
HIGH RESOLUTION ADCs

A 12-Bit 110MS/s 4-Stage Single-Opamp Pipelined SAR ADC with Ratio-Based GEC Technique

Rui Wang, U-Fat Chio, Sai-Weng Sin, Seng-Pan U, Zhihua Wang, and Rui P. Martins

FEATURES

Background Calibrated Multi-Stage Pipelined-SAR ADC
Ratio-Based Gain Error Calibration Technique
Only one PN Injection to Calibrate Multiple Gain Stages
Low Power consumption 12mW
High Sampling Rate, 120MHz
High Resolution, SNDR=63dB
Excellent Power efficiency, FoM_W=85fJ/step
Active Area, 0.12mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a 12-bit 120MS/s multi-stage pipelined SAR ADC integrated through a single low-gain op-amp. A ratio-based GEC (Gain Error Calibration) technique is proposed to reduce the complexity of digital calibration circuit. A timing-derived technique is employed to share a single op-amp for residue amplification between pipelined SAR stages, where three non-overlap phases are allocated to maximize both usable bits and op-amp amplification time in each sampling period. Only one PN (Pseudo-random Number) signal is employed to perform the dither injection but calibrate multiple gain errors, and thus accelerates the convergence speed and minimizes the analog modification due to the background calibration. The effectiveness of the architecture is verified in a 65-nm CMOS chip whose active core area is 0.12 mm^2 only. The ADC obtains a peak SNDR of 63.2 dB and SFDR of 75.2 dB at 120MS/s consuming 12mW from a 1.2-V supply. Only 40 thousand points are needed to achieve desirable SNDR with the proposed calibration technique.

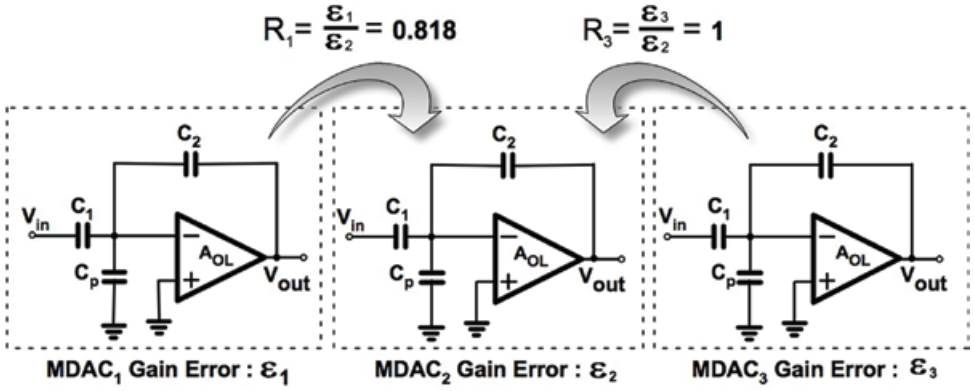

Fig. 1. Gain error ratios tracking between each MDAC.

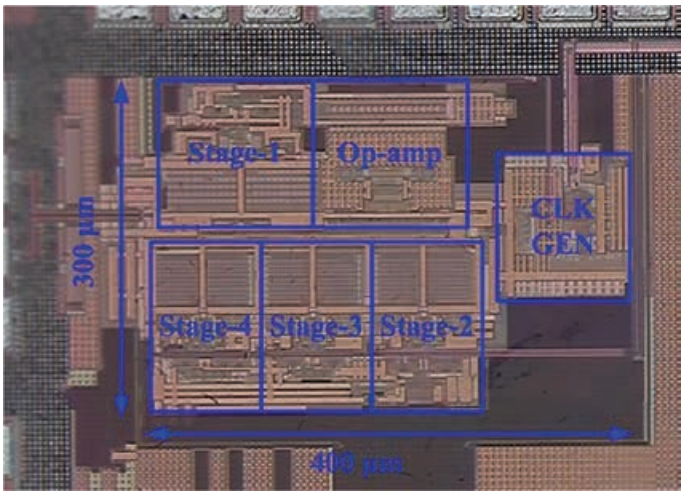

Fig. 2. Chip Photograph.

Publication(s):

[1] R. Wang*, U-Ft Chio*, S.-W. Sin*, S.-P. U*, Z. Wang, R. P. Martins*, "A 12-Bit 110MS/S 4-Stage Single-Opamp Pipelined SAR ADC with Ratio-Based GEC Technique", in Proc. IEEE European Solid-State Circuits Conference – ESSCIRC 2012, Sept 2012.

* Contributors with University of Macau

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A 22.4μW 80dB SNDR ΣΔ modulator with passive analog adder and SAR Quantizer for EMG Application

Zhijie Chen, Yang Jiang, Chenyan Cai, He-Gong Wei, Sai-Wen Sin, Seng-Peng U, Zhihua Wang, and Rui P. Martins

FEATURES

Multi-bit Sigma-Delta ADC using SAR Quantizer
Passive Analog Summation in SAR DAC Array
Very Low Power consumption 22.4μW
Sampling Rate 1MS/s
High Resolution, SNDR=80dB
Good Power efficiency, FoM_W=130fJ/step
Active Area, 0.13mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

A Feed-Forward (FF) multi-bit ΣΔ modulator with passive analog adder and 4-bit Successive Approximation (SA) quantizer is presented. The scheme is composed by two SC integrators and a 4-bit SAR quantizer with feedback Data-Weighted Averaging (DWA). The modulator covers the 10KHz bandwidth according to electromyography application. The design utilizes the same DAC array of the SAR quantizer to realize analog summation for the FF signal, which significantly reduces the power dissipation and the silicon area. The modulator operates at 1MS/s with 1V supply. The prototype chip implemented in 65nm CMOS achieves 80dB SNDR and 81dB DR with 22.4μW power consumption. The Figure of Merit (FoM) is 0.13 pJ/conv.-step.

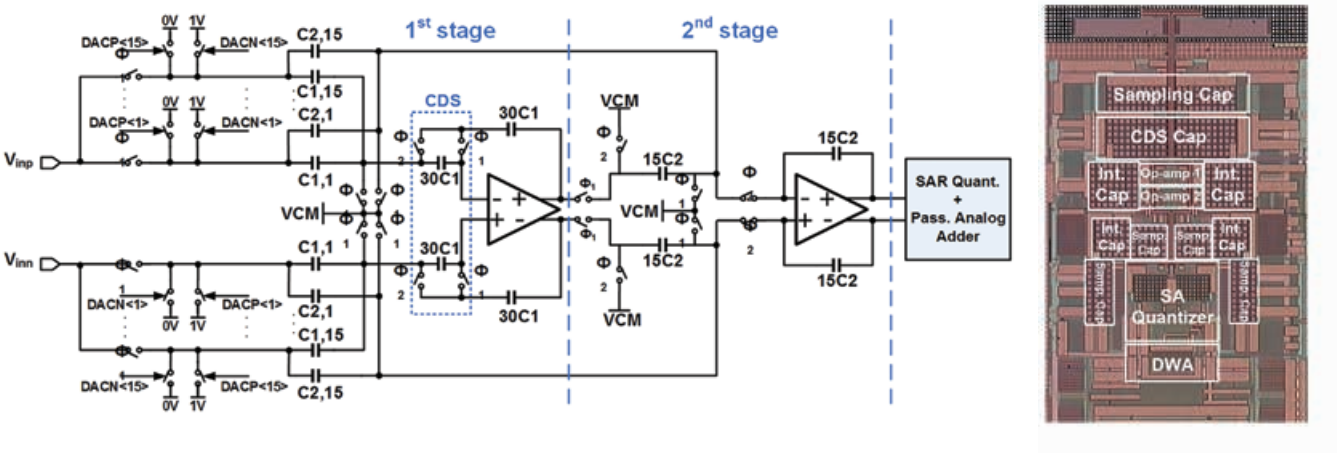

Fig. 1. Circuit Diagram of the Proposed Sigma-Delta ADC and Chip Photograph.

Publication(s):

[1] Z. Chen*, Y. Jiang*, C. Cai*, H.-G. Wei*, S.-W. Sin*, S.-P. U*, Z. Wang, R. P. Martins*, "A 22.4μW 80dB SNDR ΣΔ Modulator with Passive Analog Adder and SAR Quantizer for EMG Application", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 257-260, Nov 2012.

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A 13-bit 60MS/s Split Pipelined ADC with Background Gain and Mismatch Error Calibration

Li Ding, Wenlan Wu, Sai-Weng Sin, Seng-Pan, U, and Rui P. Martins

FEATURES

Split Pipelined ADC
Gain and Mismatch Calibration
Background Calibration
Power consumption 63.8mW
High Sampling Rate, 60MHz
High Resolution, SNDR=69dB
Good Power efficiency, FoM_W=452fJ/step
Active Area, 0.93mm^2
Silicon verified in UMC 90nm CMOS

DESCRIPTION

A comprehensive background gain and mismatch error calibration technique is proposed for split ADC, without injecting any test signal. By employing comparator threshold random selection method, the input/output transfer characteristics of each split ADC channel is differed, which allow their residue transfer curves are uncoupled and hence the calibration can be extended to any pipeline stages. Based on Least Mean Square (LMS) adaptation the interstage gain error and capacitor mismatch error are corrected. All the estimations and corrections are performed in digital domain, resulting in little analog circuit modification. The proposed calibration technique is applied on a 13-bit 60MS/s pipelined ADC. Fabricated in a 90nm CMOS process, the ADC achieves 70.8dB SNDR at a power consumption of 63.8mW. The FoM is 377fJ/ step at DC and 452 fJ/ step at Nyquist.

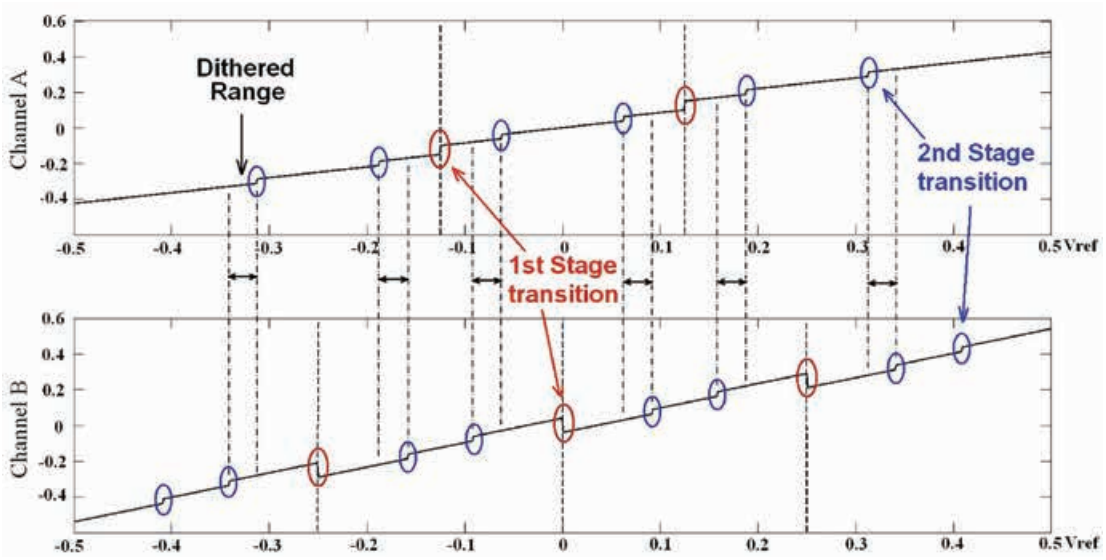

Fig. 1. Proposed Dithered ADC Transfer Characteristics.

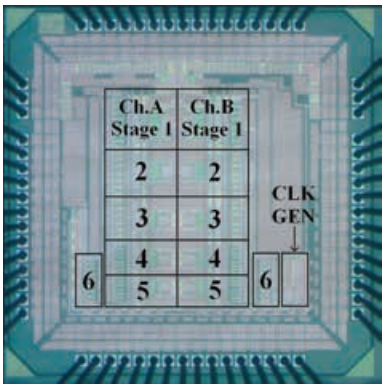

Fig. 2. Chip Photograph.

Publication(s):

[1] L. D., W. Wu, S.-W. Sin, S.-P., U, R .P. Martins, " A 13-bit 60MS/s split pipelined ADC with background gain and mismatch error calibration ", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 77-80, Nov 2013.

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Polyphase Decomposition for Tunable Band-Pass Sigma-Delta A/D Converters

Da Feng, Franco Maloberti, Sai-Weng Sin, and Rui P. Martins

FEATURES

Theoretical Analysis of the Polyphase Decomposition Technique to the NTF of Band-Pass ΣΔ modulators
Generalized and Tunable Band-Pass Implementation
Mismatch Spurs Out-of-band
Applicable to MASH structures

DESCRIPTION

The use of the polyphase decomposition technique applied to the noise transfer function (NTF) of band-pass sigma-delta (BPΣΔ) modulators is introduced and theoretically analyzed. Schemes for a second order and fourth order bandpass noise shaping are discussed in detail. The class of architectures studied here does not use resonators and avoids spur tones in the signal band. Those architectures are based on the polyphase decomposition applied only to the NTF of band-pass modulators (or to any other NTF responses). The signal transfer function (STF) remains unchanged with respect to the originating single path. The method is usable for any order but the analog inaccuracy limits its application. It is shown that an extension to MASH configurations is possible. The method allows tunability of the center frequency over a wide frequency range. Moreover, MASH schemes allow a rough-fine tuning with the rough tuning in the analog section followed by a fine digital adjustment. Simulation results verify the benefits and outline possible limits.

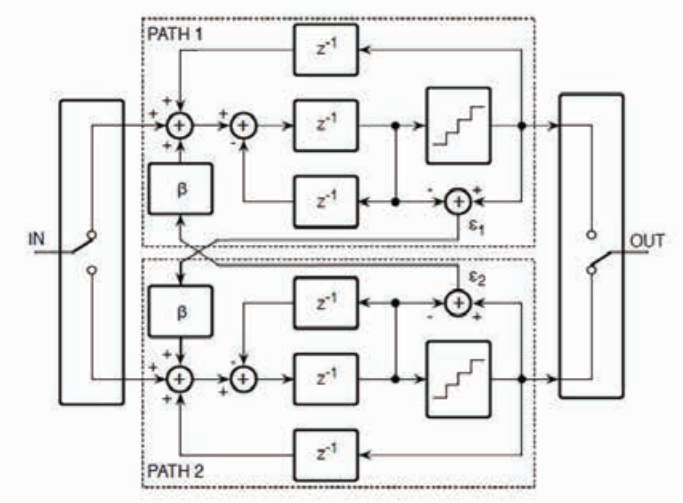

Fig. 1. A 2nd order band-pass polyphase sigma-delta ADC.

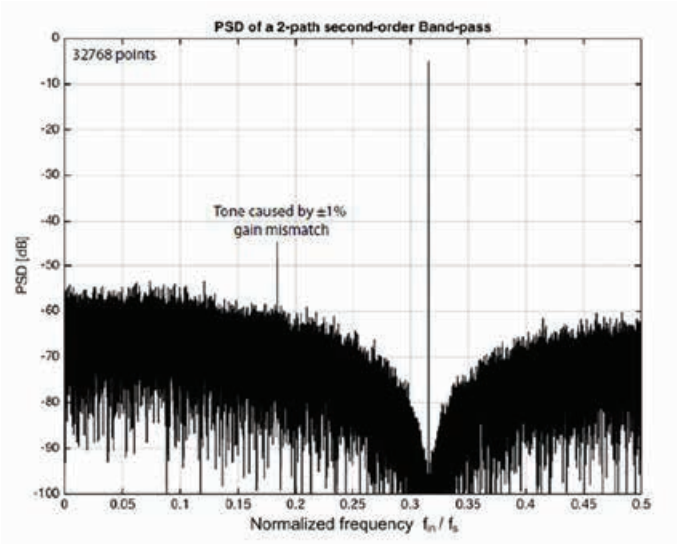

Fig. 2. FFT Spectrum.

Publication(s):

[1] D. Feng, F. Maloberti, S.-W. Sin, R. P. Martins, "Polyphase Decomposition for Tunable Band-Pass Sigma-Delta A/D Converters", IEEE Journal on Emerging and Selected Topics in Circuits and Systems, vol. 5, Issue 4, pp. 537-547, Dec. 2015.

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A High DR Multi-Channel Stage-Shared Hybrid Sigma-Delta Analog Interface for Integrated Power Electronics Controller Front-End

Yuan Ren, Sai-Weng Sin, Chi-Seng Lam, Man-Chung Wong, Seng-Pan U, and Rui P. Martins

FEATURES

Hybrid CT-DT ΔΣ Modulator with PGA Front-End
Opamp Shared in Discrete Stage
Low power consumption,68μW/Channel
High Dynamic Range, 98dB
Excellent Power efficiency, FoM_S = 179dB
Very Small Active Area, 0.03mm²/channel
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a 4-channel power electronics (PE) controller front-end interface with input signal conditioning and analog-to-digital (A/D) conversion functions for different power electronics system applications. The proposed front-end is composed of a 4-channel continuous-time (CT) and discrete-time (DT) hybrid sigma-delta modulator (H-ΣΔM) embedding an input programmable-gain (PGA) in the first CT stage in order to enhance the dynamic range (DR). The second shared DT stage is designed to utilize multiple-sampling technique with a shared single Op-Amp for low power consumption. This PE controller front-end chip is fabricated with 65 nm CMOS technology. Measurement results show a high dynamic range of 98.3 dB and 84.2 dB SNDR, while achieving a power consumption of 68 μW per channel and a FoMS of 172-179 dB due to the dynamic range boost.

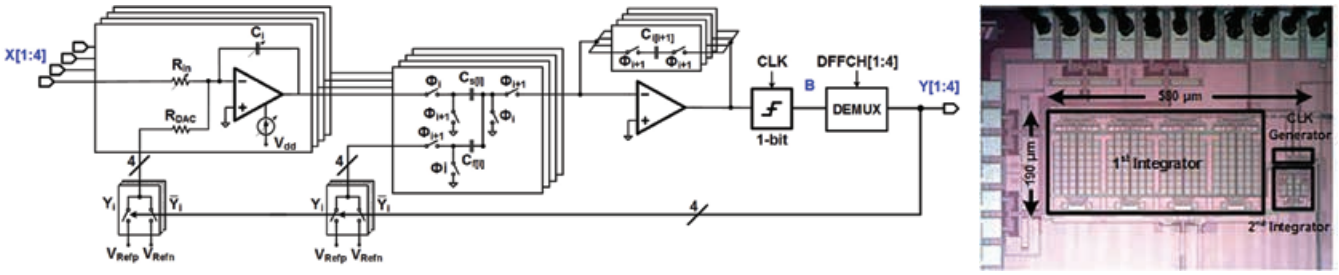

Fig. 1. The Multi-Channel Front-End Architecture and Chip Photograph.

Publication(s):

[1] Y. Ren, S.-W. Sin, C.-S. Lam, M.-C. Wong, S.-P. U, R. P. Martins, " A High DR Multi-Channel Stage-Shared Hybrid Front-End for Integrated Power Electronics Controller", IEEE Asian Solid-State Circuit Conference – (A-SSCC), pp. 1-4, Nov 2016.

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A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator with Multirate Opamp Sharing

Liang Qi, Sai-Weng Sin, Seng-Pan U, Franco Maloberti, and Rui P. Martins

FEATURES

Cascaded MASH DT-ΔΣ Modulator
Proposed Multirate Opamp Sharing Scheme
Low power consumption, 4.2mW
Wide bandwidth, 5MHz
High Resolution, SNDR=77.1dB
Excellent Power efficiency, FoM_S=168dB
Very Small Active Area, 0.066mm^2
Silicon verified in ST 65nm CMOS

DESCRIPTION

This work presents a discrete time (DT) 2-1 MASH Delta-Sigma (ΔΣ) modulator with multirate opamp sharing for Analog-to-Digital Converters (ADC), targeting the optimization of power efficiency in active blocks, like opamps and quantizers. Through the allocation of different settling times to the opamps and by adopting the multirate technique, the power of the shared opamps is utilized more efficiently, and the 4-bit SAR quantizer and the Data Weighted Averaging (DWA) in the first stage enjoy additional operation time. Moreover, a detailed analysis and related simulations are presented to validate the enhanced opamp power efficiency in the proposed sharing scheme. The 65nm CMOS experimental chip running at multirate 120/240MHz achieves a mean SNDR of 77.1dB for a 5MHz bandwidth, consuming 4.2mW from a 1.2V supply and occupying 0.066mm2 core area. It exhibits a Walden FoM of 69.7fJ/conv-step and a Schreier FoM of 167.9dB based on SNDR.

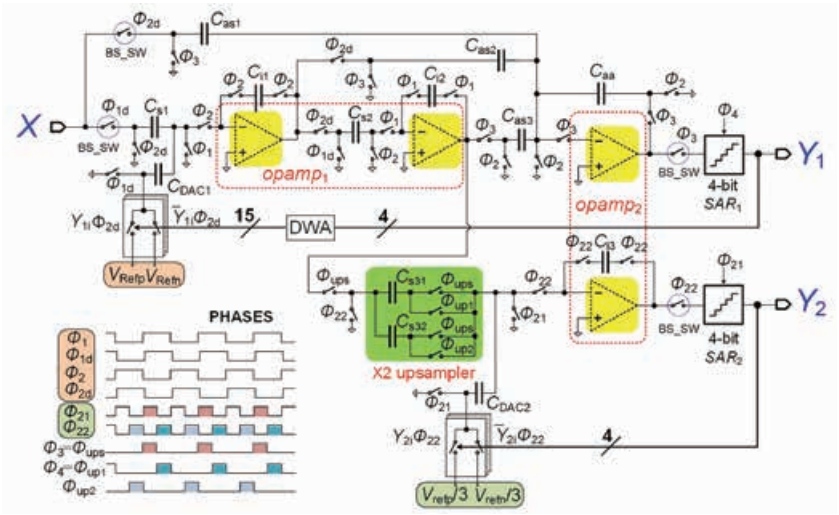

Fig. 1. ADC architecture.

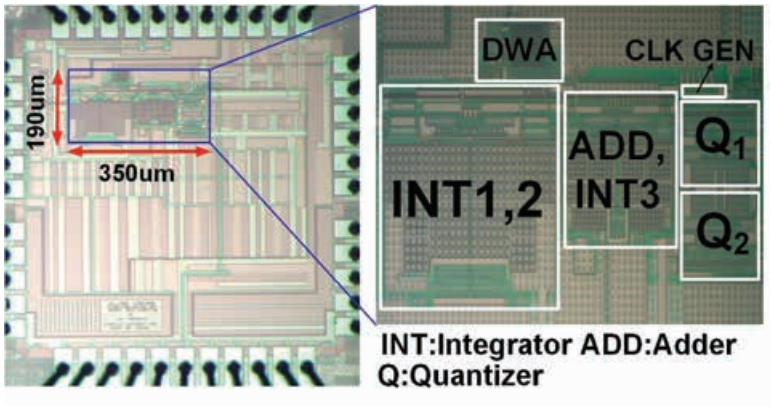

Fig. 2. Chip Photograph.

Publication(s):

[1] L. Qi, S.-W. Sin, S.-P. U, F. Maloberti, R. P. Martins, " A 4.2mW 77.1dB-SNDR 5MHz-BW DT 2-1 MASH ΔΣ Modulator with Multirate Opamp Sharing", IEEE Trans. of Circuits and Systems I – Regular Papers. in press, 2017.

[2] L. Qi, S.-W. Sin, S.-P. U, F. Maloberti, R. P. Martins, " A 12.5-ENOB 5MHz BW 4.2mW DT Multirate 2-1 Mash ΔΣ Modulator with Horizontal/Vertical Opamp Sharing in 65nm CMOS' in IEEE International Solid-State Circuits Conference, Student Research Preview, Jan 2016.

* Contributors with University of Macau

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Active-Passive ΔΣ Modulator for High Resolution and Low Power Applications

Arshad Hussain, Sai-Weng Sin, Chi-Hang Chan, Seng-Pan U, Franco Maloberti, and Rui P. Martins

FEATURES

Hybrid Active-Passive Integrator DT-ΔΣ Modulator
Proposed Positive Feedback NTF Zero Compensation
Very Low power consumption, 73.6μW
Audio bandwidth, 25kHz
High Resolution, SNDR=88.2dB
Excellent Power efficiency, FoM_S=176dB
Very Small Active Area, 0.1mm²
Silicon verified in ST 65nm CMOS

DESCRIPTION

This paper discusses the use of a Low Gain Amplifier and a Passive Switched-capacitor (SC) network to enable the SC integrator function. The method is applied to a Delta-sigma Modulator to achieve high resolution as proven by the 65nm CMOS Technology Test Vehicle. Compared to the conventional operational amplifier (op-amp) based SC integrator, this solution utilizes a low gain open loop amplifier to drive a passive SC integrator with positive feedback. Since the open loop amplifier requires a low DC gain and implements an embedded current adder, the power consumption is very low. Power reduction is obtained by using passive feedforward with built-in adder to assist the first amplifier. The low swing obtained at the output of the active blocks relaxes the slew rate requirement and enhances the linearity. Implemented in 65-nm digital CMOS technology with an active area of 0.1-mm², the test chip achieves a dynamic range (DR) of 91dB, peak signal-to-noise ratio (SNR) of 88.4dB, peak signal-to-noise-plus-distortion ratio (SNDR) of 88.2dB, and a spurious free dynamic range (SFDR) of 106dB while consuming 73.6μW in a 25-kHz signal bandwidth at 1V supply, yielding a Walden FoM of 70fJ/Conversion-Step and Schreier FoM of 176dB.

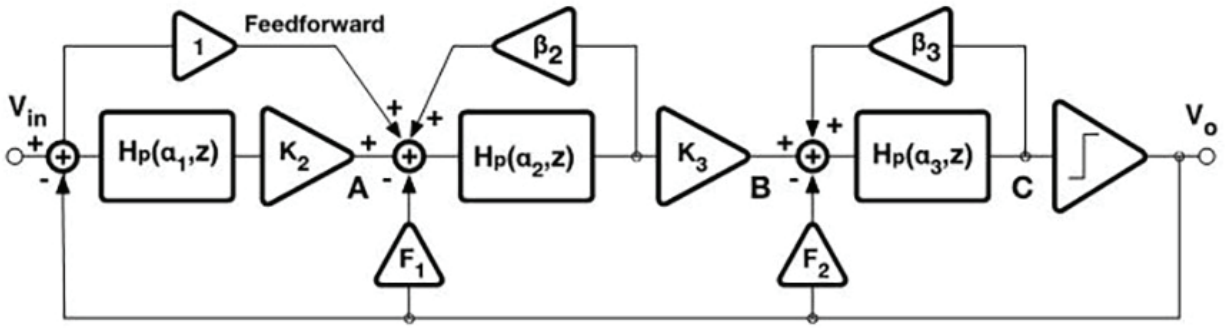

Fig. 1. ADC architecture.

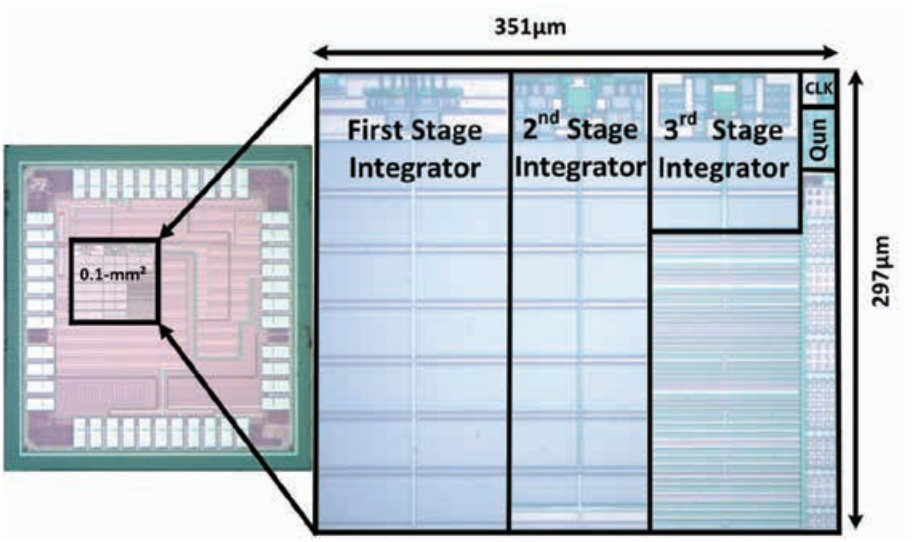

Fig. 2. Chip Photograph.

Publication(s):

[1] A. Hussain, S.-W. Sin, C.-H. Chan, S.-P. U, F. Maloberti, R. P. Martins, "Active-Passive ΔΣ Modulator for High-Resolution and Low-Power Applications," in IEEE Transactions on Very Large Scale Integration (VLSI) Systems, vol. 25, no. 1, pp. 364 – 374, Jan 2017.

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